Explicit model of thermal stress induced by annular through-silicon-via (TSV)

Fengjuan Wang\textsuperscript{a)\textsuperscript{),}} and Ningmei Yu

School of Automation and Information Engineering, Xi’an University of Technology, Xi’an, Shannxi 710048, P. R. China
\textsuperscript{a)} wfjxiao4@163.com

Abstract: In this letter, an explicit analytical model for the stress induced by annular through-silicon-via (TSV) is developed according to the classical Lamé theory. And then, the analytical model is verified by finite element method (FEM) using ANSYS software. It is shown that, 1) the error between the analytical and FEM results is less than 5.6%, which proves the accuracy of the analytical model; 2) annular TSV induces a tensile radial stress and a compressive circumferential stress in the surrounding silicon. Finally, the guidelines are given for transistor placement to prevent the performance degradation.

Keywords: annular through-silicon-via (TSV), thermal stress, explicit model, three-dimensional integrated circuit (3D IC)

Classification: Electron devices, circuits and modules

References

1 Introduction

Three-dimensional integrated circuit (3D IC) has been widely acknowledged as an effective solution to overcome the wiring limits imposed on chip performance, density, and power consumption beyond the current planar technology [1, 2]. The reason is that 3D IC can offer some important advantages, such as the much higher integrity, the significantly shortened length of interconnects, and the heterogeneous integration of various components, and so on [3]. A critical component in 3D IC is the through-silicon-via (TSV), which provides physical and electrical connectivity among the stacked dies [4].

However, conventional fully filled TSV induces thermo-mechanical stress in surrounding silicon due to the mismatch in coefficient of thermal expansion (CTE) between TSV metal and silicon, when the structure is subjected to a thermal ramp in the process flow [5]. The thermal stress can adversely affect transistor performance and reliability. Fortunately, the partially filled structure, annular TSV, induces much lower stress than the ordinary fully filled TSV [6]. The analytical model for the stress induced by annular TSV is developed in [7]. However, the model can be obtained only by resorting to computer to solve the 1st- and 2nd-order modified Bessel functions of the first kind and the second kind. Therefore, it is necessary to develop an explicit model in order to analyze the characteristics of the annular TSV-induced thermal stress easily.

In this letter, the explicit model for the stress induced by annular TSV is proposed according to the classical Lamé theory and verified by finite element method (FEM).

2 Explicit model

The annular TSV is shown in Fig. 1, which is composed of a dielectric core, surrounding metallic annuluses, and an outer oxide liner to separate TSV metal from silicon substrate. Here, $D_d$, $D_m$, and $D_l$ represents the outer diameter of dielectric, TSV metal, and oxide liner, respectively.

As the system cools down from the annealing temperature, at which it is free of stress, to the room temperature, the whole structure exhibits an unconstrained differential shrinkage. And then the radial and circumferential thermal stresses are induced into the system. The axial stresses are subject to the requirement that the resultant axial force to be zero since there is no external force on the system [8].
With these conditions, the thermal stresses in the oxide liner and TSV metal can be obtained according to the classical Lamé theory [9]

\[
\sigma_r^l = \frac{\sigma_2 D_m^2 - \sigma_3 D_l^2}{D_l^2 - D_m^2} + \frac{D_m^2 D_l^2 (\sigma_3 - \sigma_2)}{4 r^2 (D_l^2 - D_m^2)}, \quad r \in \left[ \frac{D_m}{2}, \frac{D_l}{2} \right]
\]

\[
\sigma_\theta^l = \frac{\sigma_2 D_m^2 - \sigma_3 D_l^2}{D_l^2 - D_m^2} - \frac{D_m^2 D_l^2 (\sigma_3 - \sigma_2)}{4 r^2 (D_l^2 - D_m^2)}
\]

\[
\sigma_r^m = \frac{\sigma_1 D_l^2 - \sigma_2 D_m^2}{D_m^2 - D_l^2} + \frac{D_m^2 D_l^2 (\sigma_2 - \sigma_1)}{4 r^2 (D_l^2 - D_m^2)}, \quad r \in \left[ \frac{D_d}{2}, \frac{D_m}{2} \right]
\]

\[
\sigma_\theta^m = \frac{\sigma_1 D_l^2 - \sigma_2 D_m^2}{D_m^2 - D_l^2} - \frac{D_m^2 D_l^2 (\sigma_2 - \sigma_1)}{4 r^2 (D_l^2 - D_m^2)}
\]

where \( \sigma \) represents the thermal stress; the superscripts l and m represent the oxide liner and TSV metal, respectively; \( \sigma_1, \sigma_2, \) and \( \sigma_3 \) are the radial stresses along the interfaces of dielectric/metal, metal/liner, and liner/silicon; the subscripts \( r, \theta, \) and \( z \) refer to the radial, circumferential and directions, respectively; \( r \) is the distance from TSV center to the concerned point. Similarly, the stresses in the dielectric and silicon substrate can be given directly as

\[
\sigma_r^d = \sigma_\theta^d = -\sigma_1, \quad r \in \left[ 0, \frac{D_l}{2} \right]
\]

\[
\sigma_r^s = -\sigma_\theta^s = -\frac{\sigma_3 D_l^2}{4 r^2}, \quad r \geq \frac{D_l}{2}
\]

\[
\sigma_z^s = 0
\]

where the superscripts d and s represent the dielectric and silicon substrate, respectively.

As the system cools down from the annealing temperature to the room temperature, both the elastic strain and thermal strain are generated, such that the total circumferential and axial strains can be expressed as

\[
\varepsilon_\theta = \frac{1}{E} [\sigma_\theta - \nu (\sigma_r + \sigma_z)] + \alpha \Delta T
\]

\[
\varepsilon_z = \frac{1}{E} [\sigma_z - \nu (\sigma_r + \sigma_\theta)] + \alpha \Delta T
\]

where \( \varepsilon_\theta \) and \( \varepsilon_z \) represent the total circumferential and axial strains, respectively; \( E, \nu, \) and \( \alpha \) are Young’s modulus, Poisson’s ratio, and CTE, respectively; and \( \Delta T \) is thermal load from annealing to room temperature.

The thermal stresses can then be determined from boundary conditions for the continuity of the strains at interfaces as follows

\[
\varepsilon_\theta^l \big|_{r=\frac{D_m}{2}} = \varepsilon_\theta^m \big|_{r=\frac{D_m}{2}}
\]

\[
\varepsilon_r^l \big|_{r=\frac{D_m}{2}} = \varepsilon_r^m \big|_{r=\frac{D_m}{2}}
\]

\[
\varepsilon_\theta^l \big|_{r=\frac{D_m}{2}} = \varepsilon_\theta^m \big|_{r=\frac{D_m}{2}}
\]

\[
\varepsilon_r^l \big|_{r=\frac{D_m}{2}} = \varepsilon_r^m \big|_{r=\frac{D_m}{2}}
\]

\[
\varepsilon_z^d \big|_{r=0} = \varepsilon_z^d \big|_{r=0}
\]

\[
\varepsilon_z^s \big|_{r=0} = \varepsilon_z^s \big|_{r=0}
\]

By combining Eqs. (1)–(13), the analytical models of the radial stresses along the interfaces of dielectric/metal, metal/liner, and liner/silicon are obtained.
\[ \sigma_2 = \frac{-a_2c_3d_1 - a_1c_2d_3 + a_1c_3d_2}{a_2b_1c_3 - a_1b_2c_3 + a_1b_3c_2} \]  
(14)

\[ \sigma_1 = \frac{-b_1\sigma_2 - d_1}{a_1} \]  
(15)

\[ \sigma_3 = \frac{-b_3\sigma_2 - d_3}{c_3} \]  
(16)

where, \( a_i, b_i, c_i, \) and \( d_i \) (i = 1, 2, and 3) can be expressed by Eqs. (17)~(26), respectively

\[ a_1 = E_m(D_m^2 - D_d^2)(2v_d^2 + v_d - 1) - E_d[2(D_m^2 + D_d^2) + v_m(D_m^2 - D_d^2) - 2v_mD_d^2] \]  
(17)

\[ b_1 = E_d(2D_m^2 - 2v_m^2D_m^2) \]  
(18)

\[ d_1 = E_mE_d(D_m^2 - D_d^2)(v_d(a_m - a_d) + a_d - a_m)\Delta T \]  
(19)

\[ a_2 = E_d(D_m^2 - D_d^2)(2D_m^2 - 2v_m^2D_m^2) \]  
(20)

\[ b_2 = E_d(D_m^2 - D_d^2)(v_m(D_m^2 - D_d^2) - (D_m^2 + D_d^2) + 2v_m^2D_m^2) \]  
\[ - E_m(D_m^2 - D_d^2)\left[(D_m^2 + D_d^2) + v_m(D_m^2 - D_d^2) - 2v_m^2D_m^2\right] \]  
(21)

\[ c_2 = E_m(D_m^2 - D_d^2)(2v_m^2D_m^2) \]  
(22)

\[ d_2 = E_mE_m(D_m^2 - D_d^2)(v_m(a_m - a_d) + a_m - a_d - v_m(a_m - a_d))\Delta T \]  
(23)

\[ b_3 = E_s(2D_m^2 - 2v_s^2D_m^2) \]  
(24)

\[ c_3 = E_s[v_m(D_m^2 - D_d^2) + 2v_m^2D_m^2 - (D_m^2 + D_d^2)] - E_d(D_m^2 - D_d^2)(1 + v_s) \]  
(25)

\[ d_3 = E_d(D_m^2 - D_d^2)E_s[v_m(a_m - a_d) + a_m - a_d]\Delta T \]  
(26)

Consequently, the thermal stress distributions can be obtained by substituting Eqs. (14)~(16) into Eqs. (1)~(6).

### 3 Model verification and discussion

FEM simulation was performed to verify the analytical model above by employing ANSYS software [10]. Considering the current 3D TSV technology, the parameters are selected as follows. The outer diameter of dielectric, TSV metal, and oxide liner are 6 μm, 10 μm, 10.2 μm, respectively. A thermal load \( \Delta T = -250^\circ C \) is assumed, which is the case of 25°C for the room temperature and 275°C for the annealing temperature [11]. The most common cases are studied here, i.e. Cu and SiO₂/BCB are used as the metal and dielectric materials, respectively. The physical constants are listed in Table I.

<table>
<thead>
<tr>
<th>Material</th>
<th>( \alpha ) (ppm/°C)</th>
<th>( E ) (GPa)</th>
<th>( v )</th>
</tr>
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<tr>
<td>Si</td>
<td>2.3</td>
<td>130</td>
<td>0.28</td>
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<tr>
<td>Cu</td>
<td>18</td>
<td>110</td>
<td>0.35</td>
</tr>
<tr>
<td>SiO₂</td>
<td>0.6</td>
<td>72</td>
<td>0.16</td>
</tr>
<tr>
<td>BCB</td>
<td>40</td>
<td>3</td>
<td>0.34</td>
</tr>
</tbody>
</table>
Since the bad impact of TSV-induced thermal stress is the decrease of performance and reliability of the transistor in surrounding silicon, we concern the stress distribution in silicon. Fig. 2 shows the analytical and FEM results of radial and circumferential thermal stresses induced by annular TSV. Because the Lamé theory, a kind of the 2-D solution, assumes the infinite thickness of the wafer and to be strain free in the z-direction resulting in the plane at the surface, the analytical solution is multiplied by a correction factor of 5 to fit the FEM simulation for both cases. It is shown that the average relative error of analytical solution as compared to FEM result is less than 5.6%, which proves the accuracy of the developed analytical model. In addition, the radial stress is tensile and the circumferential stress is compressive. The reason is that, Cu has a much larger CTE than silicon but a similar Young’s modulus with silicon, which results in a larger shrinkage of TSV than that of silicon.

### 4 Guidelines for transistor placement

Since the stresses can adversely affect transistor performance and reliability, no transistor is allowed to be placed within the region around TSV. It can be defined as the region with a change of carrier mobility over 5%. That is to say [11]

$$\frac{\Delta \mu}{\mu} = \Pi \times \sigma_r \times \beta(\theta) < 5\% \quad (27)$$

where $\sigma_r$ is the radial stress, $\beta(\theta)$ is the orientation factor, and $\theta$ represents the angle between stress applied by the TSV and transistor channel. $\theta = 0^\circ$ and $90^\circ$ mean that transistor channel is parallel and perpendicular to radial stress, respectively. The values of $\beta(\theta)$ and $\Pi$ can be found in [11].

By substituting Eq. (6) into Eq. (27), we can obtain the distance of transistors from TSV to prevent the performance degradation as

$$r > \sqrt{\frac{D_1^2 \Pi \beta(\theta)(b_3 \sigma_2 + d_3)}{0.2 c_3}} \quad (28)$$

According to the theory above, the critical safe distances from TSV for pMOS and nMOS devices are listed in Table II.
5 Conclusion

TSV-based 3D IC has emerged as an effective approach to enable smaller form factor, higher performance, and lower power consumption than conventional technologies. Annular TSV offers superior thermo-mechanical performance than the conventional fully filled TSV. This letter proposes an explicit analytical model for the thermal stress induced by annular TSV. FEM is used to verify the proposed model. It is shown that average relative error between the analytical and FEM solutions is less than 5.6%, which proves the accuracy of the analytical model. In addition, the radial stress is tensile and the circumferential stress is compressive. Finally, the guidelines are given for transistor placement to prevent the performance degradation.

Acknowledgments

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Table II. Critical safe distances from annular TSV. The unit is µm.

<table>
<thead>
<tr>
<th>θ</th>
<th>Cu &amp; SiO2 filled TSV</th>
<th>Cu &amp; BCB filled TSV</th>
</tr>
</thead>
<tbody>
<tr>
<td>pMOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0°</td>
<td>5.7</td>
<td>6.6</td>
</tr>
<tr>
<td>90°</td>
<td>2.6</td>
<td>3.2</td>
</tr>
<tr>
<td>nMOS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0°</td>
<td>2.1</td>
<td>2.7</td>
</tr>
<tr>
<td>90°</td>
<td>0.5</td>
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