190 GHz high power input frequency doubler based on Schottky diodes and AlN substrate

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Abstract: This paper presents the design and development of a 190 GHz Schottky-diode frequency doubler (×2 multiplier) which can handle up to 260 mW input power. In order to increase the power handling capability, a modeling approach incorporating computer-aided design (CAD) load-pull techniques to characterize the diode performance is proposed. By the use of this approach, effects of several critical diode parameters on the power handling issue are quantitatively investigated and based on the analysis, a discrete diode chip is designed for the doubler. To ensure rapid heat sink in the doubler circuitry, low cost aluminum nitride ceramic (AlN) is selected as the dielectric material of the circuit substrate, which has significantly better thermal conductivity compared with currently widely-used fused quartz. The doubler circuitry is based on a balanced configuration, which brings a merit of avoiding the use of a filter for the input and output signal isolation. The doubler circuit is optimized by co-simulation using ANSYS’s HFSS and Keysight’s ADS. The measurements show that the doubler can handle up to 260 mW input power with a power conversion efficiency of nearly 8%, resulting in 20 mW output power at 193 GHz.

Keywords: Schottky diodes, high power, CAD load-pull, AlN substrate, terahertz multiplier

Classification: Microwave and millimeter-wave devices, circuits, and modules

References
1 Introduction

Terahertz (THz) frequencies lie in the electromagnetic radiation spectrum from 0.1 THz to 10 THz spanning the gap between light and radio waves which are thought to be the least exploited electromagnetic bands primarily due to the relative immaturity of sources and detectors in terms of technical performance compared
with the microwave and optical counterparts. Given its special position in the electromagnetic spectrum, THz radiation is widely addressed in radio astronomy and atmospheric observation, and it is considered as a promising candidate for future high-speed wireless communication and security imaging [1, 2, 3].

As one of the key application enablers, THz sources have drawn considerable efforts in investigating all types of technologies to generate stable and sufficient levels of RF power [4]. Among these technologies, solid-state electronic approaches attract significant interest owing to the features of compact size, capability of room temperature operation and potential for chip integration. In this category, frequency multiplication has turned out to be the most common method to generate THz frequency signals [4]. GaAs Schottky-diode-based multipliers are extensively used to realize this function as they can yield a reasonably good power conversion efficiency and thus produce sensible output power levels for system application even without signal amplification in THz frequencies [5].

Due to the commercial availability of solid-state high power sources in W-band and the current difficulties in implementing solid-state amplifiers above this frequency range, it is a common option to use a W-band high power source to drive a multiplier chain to form a solid-state THz signal generator [6, 7, 8]. Therefore, the first multiplier is one of the key components in the chain as it is required to handle high input power so as to produce sufficient output power to drive the subsequent multipliers in the chain.

To achieve this goal, two primary technical obstacles need to be overcome, which are the power handling capability of Schottky diodes and the thermal issue associated with the high power. Since the active layer of a diode anode is normally quite thin (on the order of several hundred nanometers), it is necessary to carefully optimize the diode properties which make it capable of handling certain power level of the driven input without causing the diode catastrophic failure due to the excessive input power. For the thermal issue, high input power will lead to higher operation temperature in the diodes, which adversely affects the circuit performance or even disables the diodes [9]. To tackle these two issues, the common strategy is to use more diode anodes to share the high input power, and to adopt high thermal conductivity materials as circuit substrates for rapid heat sink, respectively [10].

For this targeted frequency band, in [11], a dual GaAs circuit substrate configuration in a single waveguide with an integrated diode structure is proposed to accommodate 12 diode anodes to handle 120 mW input power in W-band. In this work, GaAs provided modest thermal conductivity and stacking 12 anodes facilitated the input power handling as the input power on each anode is 9 mW by assuming that the input coupling is 90% (90% of the input power from the multiplier input waveguide can arrive at the diode chip.) and the power on each anode is equally distributed, however it used considerable wafer space and is thus very costly to fabricate. In [12, 13], discrete 4-anode diodes were mounted onto conventional fused quartz substrates to handle the maximum input power of 100 mW and with the same assumptions, the input power on each anode is 22.5 mW. The thermal conductivity of this quartz is poor and admittedly this can be one of the factors that limit the usage in higher power cases. However, it remains unknown whether the anode power handling capability can further be improved.
Therefore, better quantitative understanding on how diode parameters affect its power handling capability is required to clarify this issue and make the circuit design more efficiently.

To make better use of the already available driving power capability in W-band, in this paper, we present the design and development of a 190 GHz frequency doubler (×2 multiplier) featuring high input power handling capability. A modeling approach of Schottky diodes is proposed to characterize the effects of diode parameters on the power handling issue. The approach incorporating computer-aided design (CAD) load-pull techniques makes full use of simulation features offered in the CAD software [14], which provides an effective diode parameter design strategy for frequency doublers. Based on the analysis through the proposed model, a 6-anode discrete diode chip is designed for this work to handle the high power input. In order to alleviate the adverse thermal effects associated with the high input power, low cost aluminum nitride ceramic (AlN) which has excellent thermal conductivity is selected as the substrate material. The measurements show that this doubler can handle an input power up to 260 mW. The peak power conversion efficiency of 8% is obtained when the input power level is 200 mW and the output frequency is 193 GHz. When the input comes to 260 mW, the efficiency only drops slightly and this input level generates the maximum output power of 20 mW at 193 GHz with an efficiency of 7.8%.

2 Schottky diode design

The cross-section view of the geometry of a Schottky diode anode is shown in Fig. 1 [15]. Active layers (the n-GaAs layer and the highly doped n+ GaAs layer) are built on the semi-insulating (SI) GaAs substrate. The doping density of the n+ -GaAs layer is normally $5 \times 10^{18} \text{ cm}^{-3}$ which is to prevent any impurities diffusion from the SI GaAs to the n-GaAs and provide low resistance for the ohmic contact. The doping density of the n-GaAs layer is one of the key design parameters. The anode is formed on the n-GaAs layer resulting in the Schottky contact. The airbridge finger suspended over the surface channel brings the benefit of parasitic capacitance reduction.

Several parameters related to the diode chip are the factors prominently affecting the capability of power handling in frequency doublers, which are the number of anodes on the diode chip, the doping density of the n-GaAs layer ($N_d$), and the anode area ($A_a$). The n-GaAs layer is where the Schottky junction is formed. The voltage applied to the junction modulates the depletion depth within

![Fig. 1. Cross-section view of a Schottky diode anode](image-url)
the n-GaAs layer which provides the nonlinearity of a diode for frequency multiplication.

The most straightforward way to increase the power handling capability is to stack more anodes on the diode chip, but the number is limited by the physical size of the diode mounting structure which greatly affects the circuit’s electromagnetic (EM) characteristics in THz range. Another effective approach to increase this capability is to lower the \( N_d \) since this will lead to a larger reverse breakdown voltage \( (V_{br}) \). However, decreasing \( N_d \) increases the device’s resistance which will generate more power loss, resulting in lower power conversion efficiency and higher operation temperatures. For a given \( N_d \), a larger anode area \( A_a \) can handle more power, but the required embedding impedances are inversely proportional to \( A_a \) and therefore there are practical difficulties on the range of impedances that can be matched when designing the doubler circuitry for very large \( A_a \).

As a result, complex tradeoffs have to be involved although there are only a limited number of diode parameters to be determined. To design the diode chip parameters for this work, a load-pull test bench built in CAD software is proposed to give a quantitative insight of the intrinsic performance of a single diode anode. With the knowledge of a single anode’s performance, it is facilitated to determine the anode number on the diode chip to meet the design goal. For this design, the nominal input power is set to be 200 mW. As schematically displayed in Fig. 2, a standard diode model built in the Keysight’s ADS is used to simulate the nonlinear behavior of a single Schottky junction. The concerned diode physical parameters are translated into the corresponding electrical parameters which can be easily assigned to the diode model used in ADS [16]. The ideal band-pass filters (BPFs) and DC feed are components provided in ADS for necessary signal separation. The high-pass filter (HPF) and the absorption load provide a return path for the potential generation of the harmonics higher than the second one. Reverse voltage bias is applied to the diode to ensure its varactor operation. Since the diode impedances at the input and output frequencies vary along with the input power levels and the DC bias, the impedances at the input and output ports are required to
provide the optimum embedding impedance conditions to eliminate any impedance mismatch between the diode and the ports when applying different input power levels and DC bias voltages. Therefore, for a certain set of diode parameters, by adopting the load-pull techniques (e.g. tuning the input power levels, the impedances at the input and output ports and bias voltages), the best diode performance for frequency doubling can be known with the help of the harmonic balance (HB) codes offered in ADS. This can give a quick solution on what the input power should be to drive the device to yield a maximum frequency conversion efficiency under the condition of a certain set of diode parameters. In the following text, we call this power value the optimum input power.

Fig. 3a shows the simulated optimum input power on a single anode for varied anode areas at different doping densities when the nominal output frequency is set at 190 GHz. (When changing the output frequency around 190 GHz in the simulations, no significant change in terms of the performance indicated in Fig. 3 was observed.) Each optimum input power value was obtained in the load-pull simulation as a pump power level in order to result in the maximum conversion efficiency when the diode with a given Nd and Aa is presented with the optimum embedding impedances and the optimum bias voltage.

The doubler in this work is intended to adopt balanced configuration and this requires the diode chip featuring an even number of anodes, which are equally paired by number in anti-series connection (the detailed balance configuration of the doubler circuitry is presented in Section 4.). For our targeted frequency band, in order to avoid adverse EM effects brought by the diode chip physical size, the number of anodes should be no more than 6. If a 4-anode option is preferred, by assuming that the input coupling is 90% and the power on each anode is equally distributed, the power each anode handles is needed at least to be 45 mW to meet the 200 mW input requirement. According to Fig. 3a, to maintain the maximum efficiency operation at this power level, Aa has to be larger than 55 µm² for all doping densities. However, as shown in Fig. 3b, the dissipated power which directly leads to heat generation also increases as the anode area increases. Furthermore, as already stated, the very large anode area brings practical difficulties.
in designing the doubler circuitry. If we consider a 6-anode configuration, the input power on each anode comes at 30 mW with the same assumptions. From Fig. 3a and Fig. 3b, it is easy to find that a set of diode parameters with the doping density of $1 \times 10^{17}$ cm$^{-3}$ and the anode area of 45 µm$^2$ can meet the input power requirement and the dissipated power remains at a reasonable level. Table I presents the proposed diode parameters for this work. The zero-biased junction capacitance $C_{j0}$ and the series resistance $R_s$ are calculated based on the doping and anode properties [17]. As indicated in Fig. 3a, the optimum input power for this set of diode parameters is 31 mW. In the load-pull simulations, it was found that the efficiency almost remained the same as the input power increased beyond 31 mW and time-domain calculations were performed to check that the increment of the input power would not let the voltage across the anode enter the breakdown, which minimizes the risk of damaging the device. This gives adequate design margins to achieve the input power handling goal.

<table>
<thead>
<tr>
<th>Number of anodes</th>
<th>n-GaAs doping $N_d$ (cm$^{-3}$)</th>
<th>Anode area $A_a$ (µm$^2$)</th>
<th>Zero-biased junction capacitance $C_{j0}$ (F)</th>
<th>Reverse breakdown voltage $V_{br}$ (V)</th>
<th>Series resistance $R_s$ (Ω)</th>
</tr>
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<tbody>
<tr>
<td>6</td>
<td>$1 \times 10^{17}$</td>
<td>45</td>
<td>47.5</td>
<td>−14</td>
<td>7</td>
</tr>
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</table>

### 3 Substrate material selection

In order to address the thermal issue associated with the high input power level, AlN (relative permittivity = 8.8) is selected as the substrate material as it has significantly better thermal conductivity than other materials such as fused quartz and GaAs, as shown in Table II. Higher thermal conductivity provides a more rapid heat flow from the diodes to the metallic block which is vital for maintaining a modest temperature increase in the anodes and for not adversely affecting the doubler performance. Microstrip line features can be formed photolithographically on this substrate by the same approaches as on quartz.

<table>
<thead>
<tr>
<th>Material</th>
<th>AlN</th>
<th>GaAs</th>
<th>Fused quartz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal conductivity (W/m·K)</td>
<td>120</td>
<td>51</td>
<td>1.4</td>
</tr>
</tbody>
</table>

### 4 Circuitry design

The doubler circuitry is designed based on balanced configuration [18] to achieve necessary isolation between the input and output ports without employing an RF blocking filter. For this configuration, the pairs of diodes are placed in anti-series
between balanced and unbalanced transmission lines schematically shown in
Fig. 4. If the input incident power coming to the diodes at frequency \( f_0 \) is in a
balanced mode, then the output radiation at \( 2f_0 \) is generated in an unbalanced mode.
In this way, as the unbalanced line does not support a balanced mode, and
vice versa, the isolation is achieved. In Fig. 5, the whole doubler circuitry incor-
porating the balanced configuration is presented.

The input wave is incident on the diode chip in a balanced mode (TE\(_{10}\)) coming
from the reduced-height WR10 waveguide. The output frequency is generated by
the diodes in an unbalanced mode (TEM) and is free to propagate through a
suspended microstrip line based on 50 µm-thick AlN substrate. But the input wave
can also propagate beyond the diode chip towards the output end. In order to
suppress this leakage, the output radiation propagates further through a suspended
microstrip channel, which can be seen as a sufficiently width-reduced version of the
input reduced-height WR10 waveguide. In this way, the unbalanced suspended
microstrip line does not support the balanced input TE\(_{10}\) mode, which provides the
cut-off of the input TE\(_{10}\) mode and creates a reactive termination for the input
signal. Since the radiation at the output frequency is excited in TEM mode and is
not supported to propagate in a balanced waveguide, it is then coupled via a probe
transition to the output WR5 waveguide without leaking to the input port. At the
other side of the transition, the DC-bias is connected to the diodes through a low
pass filter which prevents the output power from flowing to the DC-bias port. Loop
paths are formed by wire bonds to the block at the both ends of the diode chip. The reduced-height configuration at the input and output waveguides are designed for better power coupling purpose.

With the diode parameters presented in Table I, optimum embedding impedances are found to be $(12+j88)$ Ω and $(20+j42)$ Ω for the diode at the input and output frequency respectively. ANSYS HFSS is used to calculate the EM features of each passive element in the doubler circuit, including the diode chip package, bond wires, each part of the microstrip lines and waveguides, the probe transition and the low pass filter. These elements consist of the embedding network for the diodes and are designed to meet the optimum embedding impedance requirement. Standard diode models provided in Keysight’s ADS are employed to present the nonlinear behaviors of the designed Schottky diodes by the use of the proposed parameters. The circuitry design process is based on the methodology explained in [14]. The EM calculation results are exported to ADS as Touchstone files containing S-parameter information of the embedding network, which is combined with the diode models to simulate the whole circuit performance (as schematically shown in Fig. 6) using HB codes embedded in ADS. Iterative designs are performed within these two simulators to achieve optimum doubler performance so as to determine the final circuit dimensions. The simulated doubler performance is presented in Section 5 in comparison with the measured results.

![Fig. 6. Schematic diagram of doubler performance simulation bench](image)

5 Measurement

The diodes, circuit and metallic block were fabricated at the Rutherford Appleton Laboratory. The block is based on E-plane split configuration and the AlN substrate is placed in the lower part of the block shown in Fig. 7. A K-type connector is used to feed the DC-bias voltage.

The output power test setup and bench are presented in Fig. 8 and Fig. 9. The frequency synthesizer provided frequency reference to the Quinstar power source which features functions of $\times 6$ frequency multiplication and power amplification to produce sufficient driving power for the doubler. A tunable attenuator and an
isolator were inserted before the doubler to provide power control and prevent potential signal reflection into the power source. An Erickson PM4 power meter was used to calibrated the driving power level at the isolator’s output port which was to be directly connected to the doubler’s input port after the calibration. The output power of the doubler was measured also using the PM4 power meter with the bias coming from a DC voltage source, which was used to tune the voltage applied to the diodes to achieve optimum performance at each frequency point.

With knowledge of the doubler’s input and output power values, its power conversion efficiency can be calculated. In Fig. 10a, the efficiencies along with the output frequency at different input power levels are plotted. Over 190–198 GHz, reasonable output was detected with the peak efficiency of 8% obtained at 193 GHz when the input power (P_in) was 200 mW. Fig. 10b shows the efficiencies at
193 GHz varying with respect to the input power level. It is indicated that the simulation is in good agreement with the measurement to predict the optimum \( P_{\text{in}} \) when the peak efficiency is achieved, which demonstrates the effectiveness of the diode and circuit design. From these results, it can also be observed that when the \( P_{\text{in}} \) increases from 200 mW to 260 mW, the efficiency only drops slightly. This results in that the peak output power of 20 mW appears at \( P_{\text{in}} = 260 \) mW with the efficiency of 7.8%. Fig. 11a and 11b respectively show the efficiencies and output power at \( P_{\text{in}} = 260 \) mW along with the output frequency. The measurement results are in good qualitative agreement with the simulations in terms of the curve tendency. The discrepancy in terms of output power is attributed to additional waveguide and circuit losses.

Table III summarizes the performance of published doublers in the similar frequency range based on Schottky technology. By the use of the proposed diode parameter design method incorporating CAD load-pull techniques and by adopting AlN as substrate material, the capability of power handling of the designed doubler is remarkably improved, which makes it generate more output power. Through the numerical modeling of the diode performance, a 6-anode diode chip is designed to handle up to 260 mW input power which brings a merit of less wafer space.
consumption. Furthermore, low cost AlN ceramic is demonstrated as a suitable substrate material for high power application cases in THz band. In this work, the primary goal is set to address the power handling issue with the bandwidth performance moderately compromised for the time being, but further optimization on diode geometry will make it possible to design embedding networks for better bandwidth performance.

<table>
<thead>
<tr>
<th>Table III.</th>
<th>Summary of published doubler performance in the similar frequency range</th>
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<tbody>
<tr>
<td>Ref.</td>
<td>Number of anodes</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>[12]</td>
<td>4</td>
</tr>
<tr>
<td>[13]</td>
<td>4</td>
</tr>
<tr>
<td>this work</td>
<td>6</td>
</tr>
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</table>

6 Conclusion

In this paper, a 190 GHz Schottky-diode high power input frequency doubler is presented. In order to address the power handling issue, a diode design model based on CAD load-pull techniques is proposed to quantitatively look into the effects of diode parameters on its performance. The effectiveness of the modeling is experimentally verified by good agreement between the simulation and measurement results of the doubler circuit. By adopting AlN as the substrate material for heat sinking, the 6-anode Schottky diode doubler can handle up to 260 mW input power in its operational frequency range. The peak efficiency of 8% is achieved at 193 GHz when the input power is 200 mW. The maximum output power is measured to be 20 mW also at 193 GHz with the efficiency of 7.8% when the input power is 260 mW. The results demonstrate the feasibility of AlN substrate which has superior thermal conductivity to that of conventional fused quartz to be applied in THz circuits. Moreover, the methodology of diode and circuit design presented in this work provides an effective technical approach to realize frequency multipliers featuring high power handling capability.

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