LDO regulator with high power supply rejection at 10 MHz

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Abstract: A new high-frequency power supply rejection (PSR) improvement technique is presented for a low-dropout (LDO) regulator. The proposed technique utilizes a negative capacitance at the gate of the power transistor to enhance the PSR at high frequencies by neutralizing the effect of parasitic capacitances. The simulation results show that the LDO is able to achieve a PSR of $-67.9$ dB at 10 MHz.

Keywords: low-dropout regulator, power supply rejection, negative capacitance

Classification: Integrated circuits

References

1 Introduction

Owing to the excellent power supply noise rejection, low drop-out (LDO) voltage regulators are commonly used after switching power converters in integrated power management circuits. The LDOs help provide noiseless constant voltage to noise-sensitive circuits. These days, the high power-supply rejection (PSR) of LDOs over a wide range of frequencies has become more important due to recent technological advancements, which have led to development of high-frequency operating integrated communication devices [1, 2, 3, 4]. However, the PSR performance of the conventional LDOs degrades after the dominant pole frequency of error amplifier [5]. Several advanced techniques have been developed in past to increase the PSR at high frequencies, including a replica pass transistor technique [3], which improves PSR by making the gate voltage effectively track the supply ripples, and a feed-forward ripple cancellation technique [5], which employs a feed-forward path that replicates the supply ripples at the gate of the power transistor to enhance the PSR by making power transistor overdrive voltage ripple free.

This paper presents an LDO with high PSR. The PSR at low frequencies is improved by increasing the loop gain through wide-bandwidth multiple gain stages, while the major challenge of achieving a high PSR at high frequency is realized by employing a negative capacitance circuit at the gate of the power transistor. The proposed LDO regulator achieves a PSR of $-57.9$ dB and $-67.9$ dB at 100 kHz and 10 MHz, respectively.

2 Proposed LDO with negative capacitance

At high frequencies, the power supply ripples are copied to the gate of the power transistor through the gate-to-source parasitic capacitance. An exact replica of the supply ripples at the gate can make the overdrive voltage ripple free and stop the supply ripples flow through the power transistor. However, the presence of other parasitic capacitances attenuates the ripple magnitude at the gate of the power transistor. At high frequency, the gate voltage of a conventional LDO can be given as [3]

$$v_g = \frac{C_{GS}}{C_{GS} + C_{GD} + C_P} v_{dd}$$  \hspace{1cm} (1)
where $v_g$ and $v_{dd}$ are the small-signal power transistor gate and power supply ripple voltage, respectively, $C_P$ is the parasitic capacitance of the amplifier output stage, and $C_{GS}$ and $C_{GD}$ are the gate-to-source and gate-to-drain capacitances of the power transistor, respectively. From (1), it is apparent that $v_g < v_{dd}$. This supply ripple attenuation is overcome by proposing the use of a negative capacitance at the gate of the power transistor. Fig. 1(a) shows the architecture of the proposed LDO. It consists of an Error amplifier ($A_E$), two added small-gain stages ($A_1, A_2$), a power transistor (MP), an output capacitor ($C_{OUT}$) and its equivalent series resistance ($R_{ESR}$), feedback resistors ($R_{F1}, R_{F2}$), a feed-forward capacitance ($C_{FF}$), a negative capacitance ($C_{NEG}$), and parasitic capacitances ($C_P, C_{GS}, C_{GD}$). The $C_{NEG}$ is created as a result of Miller effect established by capacitor $C_{FB}$ connected between the input and output of non-inverting amplifier $A_N$ having voltage gain of $A_{VN}$, as shown in Fig. 1(b). The value of $C_{NEG}$ can be determined by multiplying $C_{FB}$ with $(1/A_{VN})$ [6]. The negative capacitance can be achieved through this topology by utilizing a high-bandwidth (HBW) amplifier. This HBW is helpful in preventing the negative capacitance turn into the positive capacitance as the gain $A_{VN}$ decreases with frequency. Moreover, in this topology, a right half plane pole or oscillation can occur only if the total gate capacitance of LDO become negative [7]. To keep the total gate capacitance from turning negative and causing instability, the small value of $C_{FB}$ or $A_{VN}$ can be designed to satisfy the condition $C_{FF}(1 - A_{VN}) \geq -(C_{GD} + C_P)$. With the addition of $C_{NEG}$, the gate voltage of MP at high frequency can be given as

$$
v_g = \frac{C_{GS}}{C_{GS} + C_{GD} + C_p + C_{NEG}} v_{dd}
$$

$$
= \frac{C_{GS}}{C_{GS} + C_{GD} + C_p - C_{GD} - C_p} v_{dd} \approx v_{dd}
$$

Equation (2) indicate that the PSR at high frequencies can be improved, since the power transistor gate voltage can be set proportional to the supply voltage ripples by making $C_{NEG} \geq -(C_{GD} + C_P)$.

In addition, the PSR at low frequency is enhanced by increasing the overall loop gain by using an error amplifier along with two HBW small-gain stages. A feed-forward capacitor $C_{FF}$ at the output also helps to improve the PSR at low frequencies by extending the overall loop bandwidth [8, 9].

The proposed LDO design leads to five left-half-plane (LHP) poles and two LHP zeros. The dominant pole is generated at the LDO output by using a large off-
chip capacitor. The first non-dominant pole, which is located at the gate of $M_P$, is canceled by ESR zero. The second zero formed by $C_{FF}$ and $R_{F1}$ is subsequently nullified by the second non-dominant pole formed by $C_{FF}$ and a parallel combination of $R_{F1}$ and $R_{F2}$. The third non-dominant pole, located at the output of error amplifier, is placed at high frequency by increasing the bias current. The resulting reduced output resistance of error amplifier, together with minute parasitic capacitance, forms the pole at a frequency several tens of megahertz higher than the unity gain frequency (UGF) of LDO, and therefore does not affect the stability. The fourth non-dominant pole, located at the output of small-gain stage $A_1$, can be ignored as it appears at a frequency higher than 100 MHz due to small output resistance and parasitic capacitance. The LDO achieves UGF of 6.7 MHz with 50° phase margin at maximum load current of 40 mA. The phase margin increases with the decrease in load current. Fig. 2 shows the frequency response of the proposed LDO. The stability is confirmed for all process corners through simulation.

Fig. 3 shows the transistor level implementation of small gain stages $A_1$ and $A_2$. The amplifier $A_1$ is a simple small gain stage. Whereas, $A_2$ is a low output impedance Cherry-Hooper amplifier introduced in [10]. Fig. 4(a) shows the error amplifier of the proposed LDO and Fig. 4(b) shows the transistor level implementation of the non-inverting amplifier $A_N$. The gain of amplifier $A_N$ is designed to be around 9 dB by utilizing a few HBW small-gain stages. The transistors $M_5$–$M_7$ of $A_N$ form the modified Cherry-Hooper amplifier stage [11, 12]. The transistor $M_6$ helps in increasing the gain of the modified Cherry-Hooper amplifier stage by forming a current mirror with $M_1$. The HBW requirement of $A_N$ increases the overall quiescent current of proposed LDO. The performance of $A_N$ is verified by
3 Simulation results

The proposed high PSR LDO was implemented in a 0.18 µm technology provided by Magnachip. The LDO provided an output voltage of 1.6 V and 40 mA maximum load current with supply voltage of 1.8 V and external reference voltage of 1.2 V. It consumed 100–116 µA quiescent current under the 0–40 mA load current condition. A 7 µF output capacitor with 10 mΩ equivalent series resistance is used to ensure stable operation of the proposed LDO. Fig. 5 shows the simulated transient response with the load current step of 0–40 mA and rise and fall time of 10 ns. The simulated PSR at maximum load condition is shown in Fig. 6. The proposed LDO achieves −58.6 and −67.9 dB at 1 and 10 MHz, respectively. Table I shows the performance comparison of proposed LDO with previous LDO designs. It can be observed that proposed LDO achieve excellent PSR performance at high frequencies.

Fig. 4. Transistor level implementation of (a) error amplifier, and (b) amplifier $A_N$.

Fig. 5. Simulated transient response of the proposed LDO regulator

Fig. 6. Simulated PSR with and without the negative capacitance circuit
4 Conclusion

An LDO with high PSR at high frequencies is presented. The proposed LDO utilizes a negative capacitance circuit at the gate of the power transistor to improve the PSR of the LDO at high frequencies. Simulation results verify the improvement of PSR performance in the frequency range of 1–10 MHz.

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<th>[4]</th>
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<th>This work</th>
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</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.13 µm</td>
<td>0.13 µm</td>
<td>0.09 µm</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>I_{OUT} (max) (mA)</td>
<td>25</td>
<td>25</td>
<td>140</td>
<td>40</td>
</tr>
<tr>
<td>V_{IN} (V)</td>
<td>&gt;3.3</td>
<td>&gt;1.15</td>
<td>&gt;1.15</td>
<td>1.8</td>
</tr>
<tr>
<td>V_{OUT} (V)</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td>1.6</td>
</tr>
<tr>
<td>V_{DO} (mV)</td>
<td>&gt;300</td>
<td>&gt;150</td>
<td>&gt;150</td>
<td>200</td>
</tr>
<tr>
<td>I_{Q} (µA)</td>
<td>40.6–76.8</td>
<td>50</td>
<td>33–145</td>
<td>100–116</td>
</tr>
<tr>
<td>PSR at 10 MHz (dB)</td>
<td>−66</td>
<td>−56</td>
<td>−56</td>
<td>−67.9</td>
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</tbody>
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