An integrated inverted and non-inverted buck converter

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Abstract: In this paper a new topology of high step-down dc-dc converter is proposed. The proposed converter uses an interleaved structure with one phase using a traditional buck converter and the second phase uses its inverted version. By this technique a high step down voltage conversion can be achieved as compared to the traditional interleaved buck converter. Operating principle and steady state analysis of proposed converter is given. An experiment is carried out on a 25 V input, 5 V/1 A output laboratory prototype to obtain experimental results and verify the effectiveness of the proposed converter. An efficiency of 83.7% is achieved at the rated load and a maximum efficiency of 88% is achieved at 0.5 A load current.

Keywords: buck converter, interleaved, step-down voltage conversion

Classification: Electron devices, circuits, and systems

References

1 Introduction

Several applications operate at very low dc supply voltages. Some common applications are voltage regulator modules (VRM) for powering microprocessor, light emitting diode (LED) lamps and portable devices. For such applications a very high step-down dc-dc voltage conversion is required [1, 2]. For such a high voltage conversion, the conventional buck converter must operate at extremely low duty cycle which results in increased power loss [3]. For this purpose, several high step-down dc-dc converter topologies have been reported in the literature.

Interleaved buck converters (IBC) have received a lot of attention due to its low ripple characteristics. However, they do not lower the voltage conversion ratio [4]. Tapped and coupled inductor buck converter can achieve the high step down conversion ratio by using proper number of turn ratio, but there exists some leakage inductance which causes high voltage spikes on the switches [5, 6, 7]. Switched capacitor technique can provide high step down voltage without operating at low duty cycle. However, switched capacitor converter has very poor efficiency [8, 9]. Switched inductor cells are also used to achieve high step-down voltage conversion but the ripples are high due to L-switching cell [10]. To obtain a high step down voltage conversion a new topology of dc-dc converter is presented in this paper. Fig. 1 shows the circuit diagram of the proposed converter. While benefiting from the low ripple characteristics of interleaved structure it can give improved step down conversion ratio as compared to a traditional IBC.

2 Operating principle of the proposed converter

The circuit diagram of the proposed converter is shown in Fig. 1. Switches $S_1$ & $S_2$ are the active switches of phase#1 and phase#2 respectively. Similarly $D_1$ & $D_2$ are the freewheeling diodes. $L_1$ and $C_1$ are the filtering inductor and capacitor of phase#1 and $L_2$ and $C_2$ of phase#2. Inductors $L_1$ and $L_2$ are same and equal to $L$ and capacitors $C_1$ and $C_2$ are also same and equal to $C$. $C_O$ is the output smoothing capacitor, $V_S$ is the supply voltage and $R_L$ is the load resistance.

The proposed converter operates in continuous conduction mode (CCM) and its duty cycle is above 50%. The two phases of the proposed converter are operated at 180 degrees phase shift. Switches $S_1$ & $S_2$ are turned on and off by two PWM signals. The PWM signal of $S_2$ phase is delayed by 180 degrees. There are four switching states in one switching period $T_S$. Fig. 2 shows the circuit diagram of the
proposed converter in each switching state and Fig. 3 shows the steady state waveforms.

2.1 State–I (t₀ ≤ t ≤ t₁)
This state starts at time t = t₀. During state-I both the switches S₁ & S₂ are on and both the diodes D₁ & D₂ are off. Fig. 2(a) shows the circuit diagram of proposed converter in this state. The current I₁ through L₁ increases with a slope of (Vₛ-Vₒ)/L and the current I₂ through L₂ increases with slope of (Vₛ-VC₂)/L linearly. The voltage Vₐ₁ across C₁ decreases and the voltage Vₐ₂ across C₂ increases. This state ends at t₁.

2.2 State–II (t₁ ≤ t ≤ t₂):
This state begins when switch S₂ is turned off whereas switch S₁ is still on. Diode D₁ remain off and diode D₂ turns on. Fig. 2(b) shows the circuit diagram of converter in state-II. Current I₁ is still rising with the same slope of (Vₛ-Vₐ₁)/L and current I₂ decreases with a slope of −Vₐ₂/L as inductor L₂ is discharging. Voltage Vₐ₁ increases to half of the state and then decreases. Similarly, voltage Vₐ₂ further rises to half of the state and then decreases. This state ends at t = t₂ when switch S₂ is again turned on.

2.3 State–III (t₂ ≤ t ≤ t₃):
State-III is similar to state-I and again both transistors S₁ & S₂ are on and both diodes D₁ & D₂ are off. The circuit diagram is same as in state-I (Fig. 2(a)).

2.4 State–IV (t₃ ≤ t ≤ t₄):
At time t = t₃, the switch S₁ is turned off. So the diode D₁ starts conducting. Switch S₂ is still on and diode D₂ remain off. Fig. 2(c) shows the circuit diagram in this
state. During this state inductor L1 is discharging and current I1 falls with a slope of \(-V_{C1}/L\). Current I2 still rises with the same slope of \((V_s-V_{C2})/L\). Voltage \(V_{C1}\) further increases and voltage \(V_{C2}\) further decreases. This state ends at time \(t = t_4\).

3 Steady state analysis of the proposed converter

To simplify the analysis of the proposed converter, the time of each state is expressed in terms of duty cycle \(D\) and switching period \(T_S\) as \(t_0 = 0\) sec, \(t_1 = (DT_s/T_s/2)\) sec, \(t_2 = T_s/2\) sec, \(t_3 = DT_s\) sec, \(t_4 = T_s\) sec. Using the principle of volt second balance on inductors L1 we get:

\[
(V_S - V_{C1})\{(t_1 - t_0) + (t_2 - t_1) + (t_3 - t_2)\} + (-V_{C1})(t_4 - t_3) = 0
\]

Solving Eq. (1) we get:

\[
V_{C1} = DV_S
\]

By the volt second balance of L2 we get:

\[
(V_S - V_{C2})\{(t_1 - t_0) + (t_3 - t_2) + (t_4 - t_3)\} + (-V_{C2})(t_2 - t_1) = 0
\]

Solution of Eq. (3) gives:

\[
V_{C2} = DV_S
\]

The capacitors \(C_1\) and \(C_2\) are always in series with the supply voltage and therefore the output voltage of the proposed converter is given by:

\[
V_O = V_{C1} + V_{C2} - V_S
\]

From Eq. (2), Eq. (4) and Eq. (5) we get:

\[
V_O = (2D - 1)V_S
\]

As clear from Eq. (6), the voltage gain \(M\) of the proposed converter is \((2D-1)\) whereas the voltage gain of traditional interleaved buck converter is \(D\) [4]. From Fig. 3, the peak to peak ripple \(\Delta I_1\) in the current \(I_1\), peak to peak ripple \(\Delta I_2\) in current \(I_2\) and peak to peak ripple \(\Delta V_o\) in output voltage \(V_O\) can be expressed as:

\[
\Delta I_1 = \Delta I_2 = \frac{D(1 - D)V_S}{LFS}
\]

\[
V_O = \frac{(1 - D)(2D - 1)V_S}{16LCF_oF_s^2}
\]
4 Experimental results

To verify the performance of the proposed converter, the parameters shown in Table I are used to obtain theoretical and experimental results of the proposed converter. The value of filter inductor is greater than filter capacitor as in buck converter, the inductor reduces the current ripples which contributes to reduced voltage ripple at output and therefore small filter capacitor is needed [11].

For an input voltage of 25 volts and 60% duty cycle, Eq. (6) gives the output voltage which is 5 volts. The capacitor voltages are calculated using Eq. (2) and Eq. (4) and are \( V_{C1} = V_{C2} = 15 \text{ V} \). The traditional interleaved buck converter [Ref. 4] will give 15 volts output voltage from 25 volts input with same duty cycle of 60%. It can give 5 volts output from 25 volts but at 20% duty cycle which is very small. To verify the performance of the proposed converter, an experiment is carried out on a 25 V input, 5 V/1 A output prototype as shown in Fig. 4. Fig. 5 shows the experimental waveforms of the proposed converter.

| Table I. Parameters used for simulation & experiment |
|-------------------------|---------|--------|
| Name of parameter       | Symbol  | Value  |
| Input Voltage           | \( V_S \) | 25 [V] |
| Output Voltage          | \( V_0 \) | 5 [V] |
| Duty Ratio              | \( D \)  | 0.6    |
| Load Resistance         | \( R_L \) | 5 [\Omega] |
| Frequency               | \( F_S \) | 100 [kHz] |
| Filter inductor/phase   | \( L \)  | 100 [\mu H] |
| Intermediate filtering capacitor | \( C \)  | 10 [\mu F] |
| Output filtering capacitor | \( C_O \) | 10 [\mu F] |

Fig. 4. Photograph of laboratory prototype of the proposed converter

Fig. 5. Experimental waveforms of proposed converter at 60% duty cycle
Fig. 5(a) shows the waveform of supply voltage which is 25 volts and the waveforms of two pwm/gate drive signals with 60% duty ratio. Fig. 5(b) shows the waveform of the output voltage which is nearly 5 volts and waveforms of the voltages $V_{C1}$ and $V_{C2}$ which are 15 volts. From experimental results it is clear that the proposed converer can easily convert 25 V supply voltage to 5 V output voltage with an affordable duty cycle of 60% thus achieving three times higher step-down voltage conversion as compared to the traditional interleaved buck converter which will operate at very low duty cycle of 20% for achieving the same voltage conversion ratio. Hardware prototypes of the proposed converer and traditional interleaved buck converter were built and their efficiencies were measured experimentally. Fig. 6 shows a comparison of their experimentally measured efficiencies for an output voltage of 5 volts. The efficiency is plotted against load current and as clear from Fig. 6, the proposed converer can achieve 83.7% efficiency at the rated load of 1 ampere as compared to 72% efficiency of traditional interleaved buck converer.

5 Conclusions

A new two phase interleaved buck converer is presented in this study. The proposed converer is obtained by mixing a traditional buck converer to its inverted version in two phase structure. While benefiting from the existing features of interleaved converers the proposed converer has the additional advantage of extending the duty ratio by 40% as compared to traditional buck and interleaved buck converer and it avoids narrow duty cycle operation. Experimental results are verifying the effectiveness of the proposed converer. Based on its features, the proposed converer is well suited to be used as a VRM for powering modern microprocessors and other application which requires high step-down voltage conversion.

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