High-speed demonstration of low-power 1 k-bit shift-register memories using LR-biasing SFQ circuits

Toshihiro Takahashi^{a)}, Ryo Numaguchi, Yuki Yamanashi, and Nobuyuki Yoshikawa

*Dept. of Electrical and Computer Engineering, Yokohama National University,
79-5 Tokiwadai, Hodogaya-ku, Kanagawa 240-8501, Japan*

a) takahashi-toshihiro-vb@ynu.jp

Abstract: We designed a low-power shift-register memory using single-flux-quantum (SFQ) circuits for bit-serial SFQ microprocessors. In order to reduce the static power consumption of the SFQ memories, LR-biasing SFQ circuits were employed, where the resistance network for supplying the bias current is replaced with the inductance network with small resistance. We implemented a low-power 1 k-bit SFQ shift-register memory and confirmed its 30 GHz operation for all addresses. The power consumption was reduced to 26% of the conventional resistively biased SFQ memories.

Keywords: SFQ circuits, shift register, memory, superconducting integrated circuits

Classification: Superconducting electronics

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1 Introduction

The performance of present high-end digital systems based on CMOS technology is mainly limited by their power consumption. Single-flux-quantum (SFQ) circuit technology has potential to overcome the problem because of its clear advantages over the CMOS technology in terms of the high-speed and low-power operations [1]. In the realization of large-scale SFQ digital systems such as high-end SFQ computers, lack of high-density and high-speed memories, which exchange the information with microprocessors at high data rates, is one of the critical issues [2]. We are developing SFQ shift-register memories [3], which is compatible with bit-serial SFQ microprocessors [4, 5]. In the large-scale SFQ shift-register memories, however, the total static power consumption, which is dissipated in the bias resistance network, will be substantially large. This reduces the advantage of the SFQ shift-register memories in terms of the low-power consumption if we take into account the cooling cost. In order to reduce the static power consumption of the SFQ circuits, LR-biasing SFQ circuits have been investigated [6, 7], where the bias resistances for SFQ circuits are replaced with large bias inductances with small bias resistance. In this study, we developed a low-power SFQ shift-register memory using the LR-biasing technique to show its effectiveness in large-scale SFQ circuits. We designed a 1 k-bit LR-biasing SFQ shift-register memory and implemented it using the AIST advanced process (ADP2) [8]. On-chip high-speed tests were performed to examine its high-speed operation.

2 Design of low-power SFQ shift-register memories

2.1 Architecture of SFQ shift-register memories

Fig. 1 shows a block diagram of an SFQ shift-register memory that we are developing [2]. The SFQ shift-register memory consist of an array of SFQ shift registers with destructive read-out operation, an SFQ decoder, and an SFQ merge circuit composed of a tree of confluence buffers. Fig. 2 shows a block diagram of an SFQ decoder, which is composed of a tree of one-to-two SFQ switches using NDROC cells [9]. The SFQ decoder switches the data and clock into the appropriate shift register specified by the memory address.

Fig. 1. Block diagram of an SFQ shift-register memory

Fig. 2. Block diagram of an SFQ decoder

2.2 SFQ shift-registers using LR-biasing

Fig. 3 shows a circuit schematic of an LR-biasing Josephson transmission line (JTL) [6]. In the LR-biasing SFQ circuit, a large inductance L_b is inserted into the bias circuit to prevent the impulsive decrease of the bias current. The bias current is determined by $I_b = V_b/R_b$, and the static power consumption is given by $P_s = R_b I_b^2$, which can be reduced with the decrease of R_b when I_b is constant. The time constant of the bias circuit $\tau = L_b/R_b$ has to satisfy the following relationship, $\Delta t < \tau < T$, where Δt is the SFQ pulse width and T is the clock period. In the design of the LR-biasing SFQ shift register in this paper, we set the time constant to be $\tau = 5$ ps assuming that $\Delta t \sim 2$ ps and $T \sim 30$ ps. R_b was decreased to 10% of the conventional SFQ circuits so that one-tenth of power reduction can be realized. We designed and laid out an LR-biasing 64-bit SFQ shift register whose circuit area is increased by 50% compared with the resistively biased conventional JTL.

2.3 Low-power 1 k-bit SFQ shift-register memories

We designed a low-power 1 k-bit SFQ shift-register memory, which is composed of sixteen arrays of 64-bit LR-biasing SFQ shift register, a one-to-sixteen SFQ decoder, and an SFQ merge circuit composed of a tree of confluence buffers. Fig. 4 shows a microphotograph of the 1 k-bit LR-biasing shift-register memory fabricated by using the AIST 10 kA/cm² Nb advanced process (ADP2). The total bias current is about 1.3 A. The circuit is divided into two circuit blocks, each of which is biased

Fig. 3. Equivalent circuit of an LR-biasing Josephson transmission line.

separately. This will help to reduce the concentration of the bias current and the effect of the large magnetic field. We simulated the frequency dependences of DC bias margins, and obtained the sufficient DC bias margins and the maximum operating frequency of 60 GHz. At the target frequency of 30 GHz the DC bias margin is ranging from 75% to 125%. The estimated total static power consumption is 1.27 mW, which is reduced to about 26% of the conventional resistively biased 1 k-bit SFQ shift-register memories.

3 On-chip high-speed test results

We carried out on-chip high-speed tests [10] of the designed low-power 1 k-bit SFQ shift-register memory. Fig. 5 shows a block diagram of the on-chip high-speed test system, where an input 16-bit shift register (SR) and a 16-bit clock generator are connected to the input of the shift-register memory. In the test, at first 16-bit data are loaded to the input 16-bit SR by applying “Clock_In” and “Data_In” signals at low frequency. Then a “Trg_In” signal is input to the 16-bit CG to generate 16 SFQ clock pulses at high speed, which push the data on the 16-bit SR into the shift-register memory at high speed. By applying four trigger signals, 16-bit input data is shifted to the last 16-bit in the 64-bit shift register. Finally, the data in the 64-bit SR are read out by applying low-speed 16-bit “Read Clock” signals to the shift-register memory.

Fig. 4. Microphotograph of a low-power 1 k-bit SFQ shift register memory.

The input and output data waveforms when the address $(1111)_2$ is selected are shown in Fig. 6, which are measured at 30 GHz by the on-chip high-speed test. In the figure, each rising edge of the input data represents an input of an SFQ pulse and each transition of the output data corresponds to the output of an SFQ pulse. The waveforms show the correct outputs were obtained. Similarly, the correct operations were confirmed in several different input data patterns. The normalized DC bias margins of each address and circuit component measured at low frequency and 30 GHz are shown in Fig. 7, where dark and thin red bars represent the high-speed and low-speed test results, respectively. It can be seen that the DC bias margins shrunk considerably due to the internal clock skew at high clock frequency. Simulated and measured normalized DC bias margins as a function of the clock frequency are shown in Fig. 8. In this measurement, the address $(1110)_2$ is selected. One can see that measured DC margins are shrunk and shifted downward, but the overall dependence is quite similar. The maximum operating frequency by the measurement is found to be 53.3 GHz. In the on-chip high-speed tests, we confirmed the 30 GHz operation of the low-power SFQ shift-register memories for all addresses.

Fig. 5. Block diagram of a high-speed test system for the SFQ shift-register memory.

Fig. 6. Input and output data waveforms in the on-chip high-speed test when the address $(1111)_2$ is selected.

Fig. 7. Normalized bias margins of each address and circuit component measured at low frequency and 30 GHz.

Fig. 8. Normalized DC bias margins of the low-power 1-kb SFQ shift-register memory against clock frequency for the address (1110)₂. Red and blue curves are simulated and measured results, respectively.

4 Conclusion

In this study, we have designed a 1 k-bit low-power SFQ shift-register memories based on the LR-biasing technique using the AIST 10 kA/cm² Nb advanced process (ADP2), and confirmed the 30 GHz operations for all addresses. The power consumption was reduced to 26% of conventional resistively biased SFQ circuits. The result shows the possibilities of realizing large-scale SFQ circuits based on the LR-biasing technique.

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