Energy-efficient hybrid split capacitor switching scheme for SAR ADCs

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Abstract: This paper presents a newly energy-efficient switching scheme for successive approximation register (SAR) analog-to-digital converters (ADC). The novel switching method achieves zero power consumption in the first three conversion cycles. The combination of low-power monotonic and charge averaging switching method is utilized for the remaining cycles. Compared to the conventional solution, the proposed switching technique reduces the average switching energy and number of capacitors by 99.18\% and 75\% respectively. Additionally, the common mode voltage at the comparator input is in a limited variation (less than 1/8Vref).

Keywords: SAR, low-power, switching scheme, charge-averaging

Classification: Integrated circuits

References

1 Introduction

SAR ADCs are widely used in low power areas such as sensor networks and biomedical devices due to its suitability for nanometer CMOS processes. In SAR ADC designs, DAC switching is one of the major consuming source. Recently, many studies [1, 2, 3, 4, 5, 6, 7, 8, 9, 10] have been conducted to reduce the power of the DAC switching to get better energy efficiency. Compared to the conventional switching sequence, the charge averaging switching (CAS) [2] technique achieves 74.76% savings in switching energy. The Merged-capacitor switching [4] or Vcm-based [5] switching procedure has an energy reduction of 87.51% whereas the tri-level [7] and the hybrid capacitor [10] schemes achieve remarkable 96.89% and 97.66% reductions, respectively. In this letter, the proposed switching scheme consumes no switching energy in the first three comparison cycles. Moreover, a combination of charge averaging [2] and monotonic [3] switching method is adopted for the subsequent cycles. As a result, the average switching energy of the proposed switching scheme is reduced by 99.18% compared with the conventional architecture.

Fig. 1. Hybrid split capacitor switching scheme of 4-bit DAC
2 Proposed hybrid split capacitor switching scheme

Fig. 1 depicts the capacitor array structure and the switching procedure for a 4-bit SAR ADC as an example. In Fig. 1, the MSB capacitor $2C$ in red rectangular is split into $1C$ and $1C$ in parallel. Thus, the DAC array is composed of two identical sub-DAC arrays (MSB sub-array and LSB sub-array). During sampling, the differential input signals are sampled onto the top plates of the DAC, while the MSB sub-array and LSB sub-array are connected to $V_{ref}$ (high reference voltage) and $Gnd$ (low reference voltage) respectively. Then, the comparator makes first decision. If $V_{ip} > V_{in}$, the MSB sub-array capacitors on the higher voltage side are changed from $V_{ref}$ to $V_{cm}$ (half of the reference voltage), and the LSB sub-array capacitors on the other side are switched from $Gnd$ to $V_{cm}$. When $V_{ip} < V_{in}$, the switching is similar to the $V_{ip} > V_{in}$ case. In this step, the energy consumption is $-1/2CV_{ref}^2$ which means no additional energy is consumed from reference voltage. For the third bit, the capacitor array with $V_{ref}$, $V_{ref}$, $V_{cm}$, $V_{cm}$ is changed to $V_{ref}$, $V_{ref}$, $V_{ref}$, $V_{ref}$ or $V_{cm}$, $V_{cm}$, $V_{cm}$, $V_{cm}$ according to the second comparison result. The energy consumption is also zero in this bit cycle.

In [7, 10], the ADC continues with the normal monotonic switching procedure for the subsequent comparisons. To further reduce the power, the combined monotonic and charge sharing switching method is utilized. In this switching procedure, as soon as the potential of the same voltages side ($V_{ref}$, $V_{ref}$, $V_{ref}$, $V_{ref}$ or $V_{cm}$, $V_{cm}$, $V_{cm}$, $V_{cm}$) is higher, the positive side and negative side caps are merged by charge sharing. In other cases, the ADC performs with monotonic switching.

![Waveform of the proposed switching scheme](image)

Fig. 2. Waveform of the proposed switching scheme

Fig. 2 shows the waveforms at the voltage comparator inputs and common mode voltage for the first 5 phases. It can be noted that the maximum input common mode variation is $V_{ref}/8$, a value remarkably lower with respect to [3, 8].
3 Switching energy and linearity

3.1 Switching energy

The behavioral simulation of a 10-bit SAR ADC was performed in MATLAB to compare the proposed method with other recently published methods. Table I provides a comparison with the state of the art about the average energy and capacitor array area.

<table>
<thead>
<tr>
<th>Switching scheme</th>
<th>Average switching energy ($CV_{ref}^2$)</th>
<th>Energy saving (%)</th>
<th>Area reduction (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional</td>
<td>1363.3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>CAS [2]</td>
<td>344.1</td>
<td>74.76</td>
<td>50</td>
</tr>
<tr>
<td>Monotonic [3]</td>
<td>255.5</td>
<td>81.26</td>
<td>50</td>
</tr>
<tr>
<td>Vcm-based [5]</td>
<td>170.2</td>
<td>87.54</td>
<td>50</td>
</tr>
<tr>
<td>Tri-level [7]</td>
<td>42.41</td>
<td>96.89</td>
<td>75</td>
</tr>
<tr>
<td>VMS [9]</td>
<td>31.88</td>
<td>98.83</td>
<td>75</td>
</tr>
<tr>
<td>Sanyal [8]</td>
<td>21.33</td>
<td>98.43</td>
<td>75</td>
</tr>
<tr>
<td>Hybrid [10]</td>
<td>15.88</td>
<td>98.83</td>
<td>75</td>
</tr>
<tr>
<td>Proposed w/o neg energy</td>
<td>11.22</td>
<td>99.18</td>
<td>75</td>
</tr>
</tbody>
</table>

![Switching energy versus output code](image)

Fig. 3. Switching energy versus output code

Fig. 3 illustrates the simulated switching energy as a function of the output code for each technique. Compared to the monotonic switching method (255.5 CV_{ref}^2), the average switching energy with proposed method is 11.22 CV_{ref}^2 without considering the negative energy consumption which achieves 99.18% average energy reduction compared to the conventional solution. However, the negative energy is not non-physical which means that DAC gives energy back to the reference voltage sources [8]. If the negative energy is included, the average
switching energy of the proposed scheme is just \(-20.78CV_{\text{ref}}^2\), which is a remarkable reduction over previous works. Moreover, the area occupation is 75% less than what the conventional method requires.

### 3.2 Linearity

![Fig. 4. Static performance with a 10-bit SAR ADC using proposed switching method](image)

The mismatch of capacitive DAC array is a main error source which deteriorates ADC linearity. Due to process variation, the practical capacitance of each unit capacitor deviates from the nominal value. Suppose the unit capacitor is modeled with a nominal value of and a standard deviation of 1%. The simulation results of 500 Monte Carlo runs of the proposed 10-bit SAR ADC switching scheme is shown in Fig. 4, where the root mean-square (rms) of INL and DNL are depicted versus the output digital code. The worst DNL and worst INL both occurs at the \(V_{\text{FS}}/4\) and \(3\ V_{\text{FS}}/4\), where \(V_{\text{FS}}\) means the full scale signal. This proposed method has more linear transfer function in the mid-scale, which is suitable for small signal applications.

### 4 Conclusion

The novel low-power and area-efficient capacitor switching scheme for SAR ADCs is analyzed in this letter. Through combining low power switching and this new switching techniques, the proposed switching scheme exhibits better energy and area efficiency. The switching energy is 99.18% lower, and area is 75% smaller than the conventional switching technique. In addition, the static performance is also simulated and analyzed in Matlab which shows good linearity in the middle scales.