A self-adaptive write driver with fast termination of step-up pulse for ReRAM

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Abstract: Resistive random access memory (ReRAM) has been considered as a promising non-volatile storage technology of next generation especially for embedded application. However, for conventional write scheme with fixed duration and amplitude, power consumption is very high and cell performance degrades due to over-programming. In this paper, we proposed a self-adaptive write driver with fast termination of ramped-up pulse (FT-RPSWD) after write success. The slope detection and feedback mechanism are used to monitor the switching point of cell resistance. The scheme is insensitive to the selection of reference voltage, which is beneficial to ensure write margin even if the resistance variation among cells is severe. The proposed technique is verified on a 256 Kb ReRAM test macro fabricated based on 0.13-µm logic process. The mean value of endurance distribution is improved by 3 orders of magnitude from 10² to 10⁵ and the set and reset energy per bit are reduced significantly.

Keywords: ReRAM, programming, write, circuit design

Classification: Integrated circuits

References

1 Introduction

Resistive random access memory (ReRAM) has been considered as a promising nonvolatile memory of next generation with strong CMOS compatibility and scalability, especially in embedded application [1, 2, 3]. In our previous study, we showed that the switching time for both set and reset among ReRAM cells has variations in terms of voltage amplitude and duration [4, 5]. The traditional write driver scheme usually use SVP (single voltage pulse) or WVRPS (ramped-pulse series, write-verify-write) algorithm. Over-programming, including over-set and over-reset, will occur to fast cells if the write pulse duration is fixed at worst case to ensure programming success of slow cells. Consequently, power consumption is very high for those fast speed cells, especially after the resistance has been switched from high state to low one while the pulse is still on. On the contrary, un-sufficient set/reset under low voltage amplitude can’t ensure write success, no matter how long the duration is [5]. Besides, over-programming will degrade the endurance and yield [4, 6]. In our previous work, we have proved that ramped pulse is beneficial for endurance and yield [6]. In prior arts, some write scheme with feedback circuit has been put forward. But those solutions are only for write scheme with pulse of fixed duration and amplitude [3, 4, 7]. For write scheme with step-up pulses, the prior arts can’t ensure the compare circuit work during entire set operation when the pulse ramps up from low to high [8, 9]. Furthermore, the resistance variation among cells kill the sense margin when the reference voltage is fixed [10].

To address the above-mentioned problem, a self-adaptive write driver with fast termination of ramped up pulse (FT-RPSWD) after write success is proposed and verified in a 256 Kb ReRAM test chip fabricated in a 0.13-µm logic technology. The test results demonstrates that the proposed techniques can achieve low write energy and optimization of endurance.

2 Cell structure and test chip architecture

The 1-transistor 1-resistive (1T1R) memory cell structure was used in this design as illustrated in Fig. 1(a). Fig. 1(b) shows the TEM of the memory resistor structure. The integration flow is based on 0.13-µm logic process which is the same as our
previous work [11]. The cross section of the cell is shown in Fig. 1(c). After M1 formation which is used as bottom electrode (BE), the active memory layer was formed followed by the top electrode (TE, TaN) deposition. The memory resistor structure is Cu (BE)/TaxO-based storage layer/TaN (TE).

![Cell structure](image1)

**Fig. 1.** (a) 1T1R cell structure, (b) TEM of RRAM cell, (c) Cross-section view of RRAM, and (d) Function block diagram of one array.

The 256 Kb test chip consists of sixteen 32 Kb subarrays, decoder, write driver, sense circuit and some bias and control logic circuits. The detail function diagram of each subarray is shown in Fig. 1(d). The memory array based on 1T1R structure has its word-line and bit-line connected to the decoder. The write-driver provides set and reset operation to the bit-line (BL) and source-line (SL), the state of the memory cell is sensed by the sense amplifier. The control logic controls the operation of the write-driver and sense amplifier at the request of the command inputs.
3 FT-RPSWD scheme and circuit implementation

![Diagram of circuit implementation](image)

The slope detection and feedback mechanism is employed to realize FT-RPSWD circuit. Fig. 2(a) shows the circuit scheme, the voltage pulse series with controllable amplitude and duration are generated by the pulse generator which is selected by a VOL SEL signal. The cell state detector used to judge resistance switching point during write. The arbiter determines whether to cut off the write stimulus based on the feedback signal FB. Fig. 2(b) shows the detailed circuit of cell state detector. In prior art of self-terminated circuit [4], the write current has been mirrored to an Rs to form the voltage Vsample which is compared with a Vref. However, for set operation with ramped up pulse (from a small voltage to a large voltage), the Vsample is gradually increasing from a very small value to a large value. After the set operation is successful, Vsample suddenly changes to a very large value that would disable compare circuit if the Vref is simply fixed at

![Simulation results for set and reset](image)
certain value. Especially, the variation of cell resistance will kill margin between \( V_{\text{sample}} \) and \( V_{\text{ref}} \).

In our proposed circuit, a differentiator circuit is used to monitor the steep leading edge of the sample signal in order to judge the cell state. This circuit senses the current across a capacitor \( C_1 \) and uses the operational amplifier feedback resistor \( R_1 \) to develop a proportional voltage. The output from the circuit will reflect the slope of the input, not the value of input, then the sense margin will remain a large value, but not depending on the selection of the reference voltage. Capturing the signal is done using a comparator circuit designed to output a logic signal. SR latch circuit is to latch the logic signal in a steady state to be used by the terminate logic until a reset is performed.

The reset (the cell resistance from low to high) operation using step-up voltage would not have the aforementioned problems during set, because the low resistance is very small [10]. The \( V_{\text{sample}} \) will remain a relative large value until the reset operation is successful. Because it suddenly changes to a small value, the \( V_{\text{ref}} \) is easy to choose, the traditional self-terminated circuit in Ref. [4] is used during reset operation.

Fig. 2(c) and (d) show the waveforms of the proposed write driver. We can confirm that write driver is immediately cut off just after HRS (high resistance state) to LRS (low resistance state) transition and vice versa. We can also confirm that whether the written value is the same as the stored value the write driver is immediately cut off just after Write\_EN becomes high. In this way, the set and reset access time decrease respectively and wasted write energy is completely eliminated.

4 Test results and discussion

The ReRAM test chip microograph and features are shown in Fig. 3(a). The FT-RPSWD circuit test waves are shown in Fig. 3(e), the duration of set and reset step is 120 ns and the voltage step is 0.4 V. Three cases has been tested: Write 1(SET) in a high resistance state address, Write 0(RESET) in a low resistance state address, Write 0(RESET) in a high resistance address. In case one, the last step set voltage continued only 34 ns which should 120 ns in traditional write circuit; in case two, the last step reset voltage continued only 21 ns, which should 120 ns in traditional write circuit; in case three, because the initial state of the cell is in high resistance state, the write voltage directly cut off as soon as the reset operation begin. Test results show that the proposed circuit can work effectively.

The write yield has been improved from 47.3% to 95.2% by the help of the FT-RPSWD circuit as Fig. 3(c) shows. This is due to the FT-RPSWD can avoid over-programming which degrades cells performance. The set and reset energy by FT-RPSWD are reduced by 63% and 21% respectively compared with WVRPS as Fig. 3(d) shows. This is due to the FT-RPSWD can cut off the write driver after write success and skip of verify. The endurance performance of memory programming with FT-RPSWD is greatly enhanced by three orders in comparison with SVP and WVRPS as Fig. 3(b) shows. That is because the proposed circuit effectively suppressed the over-programming.
5 Conclusion

A FT-RPSWD circuit to achieve automatic write termination instead of conventional write-verify cycles for ReRAM has been proposed. The proposed circuit is verified experimentally on a 256 Kb test macro fabricated based on 0.13-µm logic process. The mean value of endurance distribution is improved by 3 orders of magnitude from $10^2$ to $10^5$. The set and reset energy per bit are reduced significantly.

Acknowledgments

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