Signal detector for 6-Gbps 55-nm CMOS Serial ATA receiver

Yongsam Moon^{a)}

School of Electrical and Computer Eng., University of Seoul, Seoul, Korea

a) ysmoon001@uos.ac.kr

Abstract: A signal detector which incorporates differential amplifiers, an RC filter, and a Schmitt trigger is designed for a 6-Gbps 55-nm CMOS SATA receiver. The differential amplifier with the increased gain and common-mode rejection ratio (CMRR) enables the signal detector to have a threshold-voltage range between 110 mV and 165 mV over all the PVT variations, which is 26.7% reduced comparing with the conventional circuit. The signal detector also has a small random threshold variation of ± 11.1 mV ($\pm 3\sigma$). The proposed signal detector is designed and verified using a 55-nm CMOS technology.

Keywords: signal detector, Serial ATA, PVT variations

Classification: Integrated circuits

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1 Introduction

As Serial ATA (SATA) is widely used in industry, the data rate passes 1.5 Gbps/3 Gbps and reaches 6 Gbps [1]. SATA has several unique features uncommon in most serial protocols. For example, out-of-band (OOB) signaling between SATA host and device (e.g. hard disk drive) go through two pairs of differential wires, providing reset and speed negotiation services between the two partners [1, 2, 3].

OOB signals are sequences of data bursts interspersed with common-mode idles as shown in Fig. 1(a). The data bursts are generally composed of repeated “00110011” patterns, where one unit interval (UI) is around 666.67 ps ($= 1/1.5$ Gbps), regardless of the operating data rate. A burst of “00110011” patterns in 1.5-Gbps data rate is equivalent to a square wave with a period of 2.66 ns. All data rates shall use the 1.5-Gbps OOB burst speed, establishing a single requirement for a signal detector.

The differential signal level of the data bursts is above 200 mVppd (mV peak-to-peak differential) and that of common-mode idles is below 75 mVppd [1]. SATA-compatible devices can detect differential voltage levels to discern the presence and absence of the data signal using a signal detector. By evaluating the time duration of these patterns, the SATA host and device can determine the meaning of the received OOB sequence without having an established serial link.

A signal detector receives the high-speed input data, detects whether a signal is valid, and generates an indication signal, *signal* as shown in Fig. 1. The input-to-output relationship of a signal detector is shown in Fig. 1(a). If the peak-to-peak

Fig. 1. (a) Input-to-output relationship of a signal detector and (b) block diagram of a 6-Gbps SATA receiver.

differential voltage amplitude is larger than a squelch threshold V_{TH} , *signal* will be ‘1’. Otherwise, *signal* will be ‘0’.

The usages of a signal detector can be classified into two categories: initialization and loss-of-signal (LOS) detection. For initialization, according to a predetermined routine, a transmitter generates a data stream and a receiver decodes the data as amplitude modulation keying [1, 2, 3] as mentioned above. On the other hand, if a receiver is floated or a transmitter is disabled, the input amplitude will reach a minimum, which is expected to be less than V_{TH} , thereby resulting in *signal* being ‘0’. If this ‘0’ state of *signal* is maintained for a certain time, it will be interpreted as LOS [4].

The input-to-output relationship of a signal detector is considerably affected by the PVT variations as well as a random variation induced by device mismatches. So, the SATA standard separates the upper bound V_{TH} of 200 mV and the lower bound V_{TH} of 75 mV [1]. It implies that a signal detector can have any output status for an input voltage swing between both the bounds.

In order to minimize the wire capacitance of the receiver’s input signals (*inp* and *inn*) for high speed operation, it is desirable to integrate an equalizer and the signal detector in a pad with termination resistors and ESD protection circuits as shown in Fig. 1(b). So, the area reduction is also important. In this paper, we propose an area-effective, high-speed signal detector for a 6-Gbps SATA receiver. The proposed signal detector utilizes differential amplifiers for lower process, voltage, and temperature (PVT) variations.

The next section of this paper discusses conventional signal detectors. Section 3 presents the proposed signal detector. Section 4 concludes and summarizes this paper.

2 Conventional signal detector

A conventional signal detector utilized a common-source (CS) amplifier with a source degeneration resistor [5]. However, since such a degenerated CS amplifier has a low voltage gain, it may not be useful when a high-frequency small-swing input data is received.

In contrast, another conventional signal detector [6] utilized two high-gain CS amplifiers without source degeneration. The first CS amplifier consists of an

Fig. 2. A conventional signal-detector circuit [6].

Fig. 3. (a) Simulated waveforms in the typical corner and (b) measured threshold voltages of a conventional signal detector [6] with the PVT variations.

amplifying transistor Q_5 and a current-source load Q_7 as shown in Fig. 2. The other CS amplifier consists of Q_6 and Q_8 . The DC biasing of the circuit is set up in order that I_{Q_5} (or I_{Q_6}) is larger than I_{Q_7} (or I_{Q_8}) and Q_{10} (or Q_9) is turned off when the differential input is zero or smaller than $0.5 \times V_{TH}$ [6].

If the differential input (V_{diff}) is larger than $0.5 \times V_{TH}$, the voltage of a node sp rises and I_{Q_5} gets smaller than I_{Q_7} . After that, Q_{10} is turned on and $sigval$ becomes ‘1’. Therefore, by means of the transistor sizing of Q_5 and Q_7 , the first CS amplifier induces an intentional voltage offset of $0.5 \times V_{TH}$. In the same way, if the differential input (V_{diff}) is lower than $-0.5 \times V_{TH}$, the voltage of a node sn rises and I_{Q_6} gets smaller than I_{Q_8} . Thereafter, Q_9 is turned on and $sigval$ becomes ‘1’. The second CS amplifier gives a negative voltage offset of $-0.5 \times V_{TH}$.

This signal detector is tested in a 55-nm CMOS technology. Fig. 3(a) shows simulated waveforms of the input and output in the typical corner, where the signal level of data bursts is 150 mVppd. In a scaled-down (e.g. 55-nm) CMOS technology, the maximum operation frequency of transistors is high enough. Therefore, the signal detector can handle data bursts with a period of 2.66 ns without too much difficulty.

However, the signal detector suffers from considerable PVT variations as shown in Fig. 3(b). The threshold voltage has a range between 100 mV and 175 mV. The large PVT variations are due to the fact that the above-mentioned two CS amplifiers are not differential amplifiers but just two individual single-

Fig. 4. (a) Proposed signal-detector circuit and (b) its simplified circuit.

ended amplifiers. Taking the output in a single-ended manner has two major disadvantages. The voltage gain is halved [7, 8]. And the DC biasing may be disturbed with the PVT variations.

3 Proposed signal detector

The issues of conventional circuits are addressed by the proposed signal detector shown in Fig. 4. The proposed signal detector utilizes two differential amplifiers as shown in Fig. 4(a). The first amplifier has a differential pair formed by transistors $M5$ and $M6$, loaded by a current mirror formed by transistors $M7$ and $M8$. The other differential amplifier consists of $M9$, $M10$, $M11$, and $M12$.

Since the gate width (W_{M8}) of a transistor $M8$ is designed to be larger than the gate width (W_{M7}) of a transistor $M7$, I_{M8} is larger than I_{M6} and $M13$ is turned off when the differential input is zero or smaller than $0.5 \times V_{TH}$. If the differential input (V_{diff}) is larger than $0.5 \times V_{TH}$, the voltage of a node tp rises and that of a node tn falls, leading to I_{M6} being larger than I_{M5} . Through the current mirror ($M7$ and $M8$), the voltage of a node xp rises, $M13$ is turned on, and *sigval* becomes ‘1’. Therefore, by means of the transistor sizing of $M7$ and $M8$, the first differential amplifier induces an intentional voltage offset of $0.5 \times V_{TH}$. In the same way, the second differential amplifier exhibits a negative voltage offset of $-0.5 \times V_{TH}$ since its input connections are interchanged.

Since the data bursts generally have repeated “00110011” patterns and positive input signals have the same magnitude as negative input signals, either of the amplifiers can be removed. The designed signal detector incorporates one differ-

Fig. 5. Measured threshold voltages of the proposed signal detector with the PVT variations.

ential amplifier, an RC filter, and a Schmitt trigger as shown in Fig. 4(b). As long as the differential input voltage (V_{diff}) is larger than $0.5 \times V_{TH}$, the amplifier turns on a transistor M_{13} . If the turn-on current of M_{13} is larger than the pull-up current of a resistor R_s , the voltage V_f will decrease. The capacitor C_s and the resistor R_s low-pass filter the unwanted high-frequency components of V_f . The following Schmitt trigger eliminates a glitch-induced ringing problem with its inherent hysteresis [9].

The proposed signal detector is designed in a 55-nm CMOS technology. The proposed circuit consumes $364 \mu A$ with a 1.2-V supply voltage and occupies $22.6 \mu m \times 18 \mu m$. With the PVT variations, threshold voltages of the signal detector are measured as shown in Fig. 5. The threshold voltage has a range between 110 mV and 165 mV. While the measured threshold voltages of the conventional circuit show the considerable dependency on the PVT variations as shown in Fig. 3(b), those of the proposed circuit simply show the dependency on the temperature variation and the process/voltage variations are quite suppressed as shown in Fig. 5. As a result, comparing with the conventional design in Fig. 2, the proposed design shows 26.7% less (or 20-mV less) PVT variations. The reduced variations are due to the increased gain (by a factor of 2) and the increased common-mode rejection ratio (CMRR) of the differential amplifier [7, 8].

Monte-Carlo simulations show that the threshold voltage has a random variation of ± 11.1 mV ($\pm 3\sigma$) due to device mismatches. The primary sources of the random variation are the input transistors (M_1 and M_2), which coincides with common knowledge [10].

According to growing interest and trend to integrate the system into a single chip using scaled-down technology and low supply voltage, the chip performance can be degraded due to IR drop, power-supply fluctuation, input-package parasitics, and so on. If voltage noises induced by such factors are considered as well as ± 11.1 -mV random variation, the threshold voltage range with the PVT variations needs to be minimized. Therefore, the 26.7% (or 20-mV) reduction of the threshold voltage range is too importance to be ignored.

4 Conclusions

A signal detector which incorporates differential amplifiers, an RC filter, and a Schmitt trigger is designed for a 6-Gbps 55-nm CMOS SATA receiver. The

differential amplifier with the increased gain and CMRR enables the signal detector to have a threshold-voltage range between 110 mV and 165 mV over all the PVT variations, which is 26.7% reduced comparing with the conventional circuit. The signal detector also has a small random threshold variation of ± 11.1 mV ($\pm 3\sigma$).

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