Errata

In Vol. 14, No. 10, 20170053, the following reference should be added after Ref. [15] as follows.


And the following editorial correction has been found and should be corrected as follows.

Wrong

Based on this point, some techniques have been proposed to reduce the frequency and overhead of DRAM refresh [1, 3, 4]. However, these retention-aware refresh approaches require either OS-level involvement, or memory controller participation, or DRAM devices modification, which results in great difficulties at implementation level.

Correct

Based on this point, some techniques have been proposed to reduce the frequency and overhead of DRAM refresh [1, 3, 4]. However, these retention-aware refresh approaches require either OS-level involvement, or memory controller participation, or DRAM devices modification, which results in great difficulties at implementation level. Research [16] proposed a hybrid memory comprised of a big SCM and a little DRAM to reduce the refresh power, but some further efforts must be took to offset the relatively poor read and write performance of SCM.