A single event transient detector in SRAM-based FPGAs

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Abstract: This paper presents a novel single event transient (SET) measurement circuit in SRAM-based field programmable gate arrays (FPGAs). Experimental results demonstrate that the new pulse detector is able to on-chip measure bipolar pulses with a detection limit of near 150 ps, compared with existing pulse detectors, detection capability and detection precision are effectively improved.

Keywords: single event transient, pulse detector, on-chip measure, SRAM-based FPGAs

Classification: Integrated circuits

References


1 Introduction

Single event transients (SETs), voltage disturbances generated when particles strike sensitive nodes [1], may propagate through the logic and eventually be latched, leading to behavioural errors of affected circuits [2]. As technology shrinks and operating frequencies increase, SETs are an ever-increasing issue for integrated circuits (ICs) adopted in safety-critical applications [3, 4, 5, 6].

Since radiation sensitivity of configuration SRAM bits is more significant than SETs in look up tables (LUTs) and wires, SETs are not main source of soft errors in SRAM-based field programmable gate arrays (FPGAs) [7] and thus have been rarely studied. However, an in-depth understanding of SET phenomena in SRAM-based FPGAs is of great value, which can provide us a good preference for accurate analysis of SET phenomena in advanced technologies (the technology nodes SRAM-based FPGAs adopted include 40 nm, 28 nm, 20 nm, 16 nm and so on).

For the sake of accurately studying SET in FPGAs, recently, researchers tend to investigate SET phenomena with the aid of actual transient pulse rather than simulation model [8]. One key technique in observing realistic SETs is pulse measurement which involves multiple parameters, e.g. detection limit, precision, area overhead and so on. Based on vernier technique, our group proposed an electrical pulse measuring circuit in [9] shown in Fig. 1, which can on-chip (avoiding pulse distortion when pulses propagate through IO logic) measure SETs with a temporal resolution of near 80 ps and detect transient pulses low to about 300 ps.

Although the pulse detector works well, it requires further improvements due to several facts. Firstly, the SET detector merely can measure one-polarity pulses, either positive pulses (0-1-0) or negative pulses (1-0-1), and double logic resources are required (high area overhead) in two-polarity case, i.e., sometimes positive SETs and sometimes negative SETs. Secondly, according to [10], when using Krypton ions with a LET of 40.2 MeV-cm²/mg, radiation induced SETs in commercial 65 nm bulk CMOS process approximately range from 0 to 500 ps, and in similar scenario, detection capability of more than 300 ps is obviously insufficient. The last but not the least, there are several deficiencies in calibration.
In this paper, we mainly present four aspects of improvements on our previously proposed pulse detector: 1) the minimum measurable pulse width is reduced to near 150 ps; 2) detection capability is extended from single polarity to dual polarities; 3) calibration circuit is modified in order for a more accurate calibration result; 4) vernier interval is adjusted to improve measurement precision.

2 Proposed improvements

As shown in Fig. 1, the SET measuring circuit mainly consists of two parts, i.e., SET capture part and edges chasing part. At first, SET is captured by LUT3 and then drives two positive edges in a time interval of pulse width (the edge in slower chain is ahead) to propagate through two chains. Then the edge in faster chain will chase after the other one in slower chain, and the comparison results stored in RS cells can precisely demonstrate the time node when the two edges cross, namely, the number of delay stages required for the two edges to meet. Thus we can determine SET width: vernier interval (Delay1-Delay2) multiplied by the number of flipped RS cells. In the following, several drawbacks in previous pulse detector and corresponding improvements are investigated in detail.

Measurable pulse width, namely, pulse width can be captured, is determined by the delay of LUT feedback path, i.e., loop path (dotted line marked in red in Fig. 1), its nominal delay is a sum of 244 ps and 70 ps (the delay of LUTs [11]). Therefore, pulses in width of less than 300 ps are probably unmeasurable. For the sake of improving the detection limit (i.e., minimizing loop path), LUT structure and routing resources were deeply studied. Fig. 3a shows a basic LUT structure, from which we know that A1 is the farthest input and A6 is the closest input from LUT6 output. Because of this, loop path is configured to propagate through A6 in previous pulse detector. In addition, a common phenomenon is that LUT output routed to other LUTs is prior to its own inputs, for instance, nominal delay of B to LUT3-A6 is 244 ps, greater than the delay of B to LUT2-A6 (125 ps).
To reduce loop path, previous LUT3 were replaced with two cross-coupled LUTs (LUT5 and LUT4) shown in Fig. 2, then the delays of outputs to inputs (wires marked in red) were routed to about 120 ps, making loop path being about 190 ps (120 ps + 70 ps). It should be noted that the two LUTs must be driven simultaneously (466 ps and 468 ps). In addition, pulse broadening technique (see LUT5-A1 and LUT5-A3 or LUT4-A1 and LUT4-A3) was applied to further improve the detection limit, which is illustrated in Fig. 3b. Optimized with the two steps, new pulse detector can measure SETs low to 150 ps (see experimental results).

To raise resources utilization efficiency, capturing two-polarity SETs in one pulse detector was proposed. Firstly, we introduce a concept of basic level (i.e., 0 for positive pulses and 1 for negative pulses). Then a latch is added to store the value shown in Fig. 2. When setting Clear to 1, signal A state is stored by the latch as basic level, based on which, SET capture part is able to capture corresponding polarity pulses. Since clear operation is demanded before each measurement, at that time pulse detector will automatically adjust to measured polarity state, making new pulse detector able to measure pulses in different polarities.

Fig. 2. Mechanism and waveform of new pulse detector.

Fig. 3. a) Basic LUT structure; b) Diagram of pulse broadening technique.

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Because core voltage, temperature, and process variation significantly affect the delays in LUTs and routing resources, pulse detector needs to be calibrated before each experiment. As shown in Fig. 1, when setting Clib to 1, both chains are configured as two ring-oscillators (ROs), and then vernier interval can be calculated out (two chains delay difference divided by the number of delay stages). However, a shortage is that although two returned paths (wires marked in blue) are manually routed to same length (3070 ps and 3071 ps reported in the Post-Place & Route Static Timing), their actual delay difference induced by manufacturing variation may be up to 300 ps (fluctuations up to 10% [9]), result in an inaccurate calibration result. To settle this issue, single returned path (wire marked in blue in Fig. 2) was presented, effectively increasing calibration precision.

According to [9], when configuration is correct and reference clock is 300 MHz, temporal resolution of SET generating circuit is about 52 ps, while previous vernier interval actually is near 80 ps, it is obviously not appropriate. So two delay stages were rerouted to a nominal delay difference of 51 ps shown in Fig. 2 (actually about 30 ps, see Table II), effectively improving detection precision.

3 Experimental results

In the paper, main experimental platform is ML605 evaluation kit (xc6vlx240t-1ffg1156) and Table I reports the logic functions of three LUTs in new pulse detector. For the sake of accurately evaluating the SET measuring circuit, previous SET generating circuit [9] was applied to the validation process. Three widths (i.e., 150 ps, 300 ps, and 450 ps) with two polarities (‘-’ indicates negative polarity) were produced and then fed into the pulse detector to validate above improvements. In the experiments, each data is measured 1000 times to make experimental results strong. To verify the robustness of pulse detector against both process variation and core voltage (here temperature is not taken into account due to its little effect in [9]), experiments were made at five scenarios (temperature is 25 degrees Celsius): 1) chip 1 at 1 V; 2) chip 1 at 0.9 V; 3) chip 1 at 1.1 V; 4) chip 2 at 1 V; 5) chip 3 at 1 V.

As can be seen in Table II, calibration after setting a new evaluation scenario is quite necessary due to the fact that the parameters including core voltage and process variation have a significant effect on vernier interval, which multiplied by average number of flipped RS cells is measured pulse width. The last column reports deviation rate between produced pulses and measured pulses. It is clear that calibration part works well and the new pulse detector can on-chip measure bipolar pulses with high temporal precision (near 30 ps), low detection limit (about 150 ps), and nice dependability (apply to different situations). It should be noted that the delay of loop path is increased when lowering core voltage, thus the detection limit is increased, i.e., narrow pulses are likely to be unmeasurable (chip 1 at 0.9 V, 150 ps).
4 Conclusion

The optimization for SET measurement circuit in SRAM-based FPGAs is presented. After the improvements, new SET detector is able to on-chip measure bipolar pulses with a detection limit of near 150 ps and a high detection precision, which are validated by subsequent experiments.

Acknowledgments

This work is supported by the National Natural Science Foundation of China under grant nos. 61674048, 61604001, 61371025, and 61574052.