A novel SEU hardened SRAM bit-cell design

Tiehu Li¹,²a), Yintang Yang¹, Junan Zhang², and Jia Liu²
¹ School of Microelectronics, Xidian University, Xi’an 710071, China
² Science and Technology on Analog Integrated Circuit Laboratory, Chongqing 400060, China
a) tiehuli@163.com

Abstract: An improved single event upset (SEU) tolerant static random access memory (SRAM) bit-cell with differential read and write capability is proposed. SPICE simulation suggests a more than 1000 times improvement of the critical charge over the standard 6T SRAM cell. With the SEU robustness greatly enhanced at low area and electrical performance costs, the proposed cell is well suited to harsh radiation environment applications such as aerospace and high energy physics.

Keywords: SRAM, single event upset, radiation hardening by design

Classification: Integrated circuits

References

1 Introduction

The data memory components have played an increasingly important role in modern electronic systems, especially in those working in harsh radiation environments. The SRAM cells are one of the most extensively used memory devices. With technology scaling down, the feature size of transistors shrinks and the distance between transistors decreases dramatically. Meanwhile, the operation voltage reduces, less charge required for logic High level representing [1]. The advancement of technology has made SRAM cells more vulnerable to high energy ion strikes due to charge sharing and enhanced charge collection by parasitic bipolar effect [2]. Charge collection at sensitive nodes of SRAM cells may cause changes of stored data, namely SEU, which brings significant computation errors in subsequent operations.

To mitigate the single event vulnerability, a number of SEU hardened SRAM cells have been proposed. The Quatro-10T cell [3] in Fig. 1(a) was proposed for promising low voltage and low power applications, but researches have pointed out that this cell suffers from high write failure probability under process and temperature variations, impeding the application of this SRAM bit-cell [4]. In addition, some inner nodes of this cell are not robust enough and its critical charge is only 3 times that of the standard 6T cell [5]. A 18T cell [6] in Fig. 1(b) and a 14T cell [5] in Fig. 1(c) were proposed later. The 18T cell features a relatively higher critical charge compared to the well-known ROCK cell, WHIT cell, LIU cell and Quatro-10T cell while at the expense of larger power consumption and area cost. The 14T cell achieves better electrical performances and lower area cost, but the critical charge is by no means preferable to the 18T cell. Along came some other designs [7, 8, 9], however, the SEU hardening capabilities of these cells are not satisfactory enough.

In this paper, a novel SEU hardened SRAM bit-cell with differential read and write capability is proposed. By delicate design of the circuit structure, the SEU tolerant capability is significantly enhanced with low area and electrical performance costs.

2 Proposed SEU tolerant SRAM cell design

The proposed SEU tolerant SRAM cell design is shown in Fig. 1(d). Two cross coupled transistor pairs P1~P4 and N3~N6 form two data latch nodes creating spatial redundancy of data. The driving transistors for each data latch node, i.e. N1~P2, N2~P3, N5~P6 and N4~P5, provide data latch paths and cross coupling between two data latch pairs, which helps storage node recover to its original value at the existence of ion hits.

First, the write and read operation of the proposed SRAM bit-cell is checked. During the write operation, the Bit Lines (BL and BLB) are driven to High/Low
logic values once the Word Line (WL) is pulled High. The differential data is written into latch pair N3~N6 at nodes Q1 and Q1B. Then Q1 and Q1B open driving paths for data latch pair P1~P4, and the input data is duplicated at storage nodes Q2 and Q2B as well. The data is stored stably by positive feedback structure in this data cell. During the read operation, Bit Lines are precharged to logic High. When WL pulls High, the logic Low data connected Bit Line (BL or BLB) is discharged to logic Low voltage, and the other Bit Line remains logic High. The resulting differential voltage between Bit Lines is detected by the sense amplifier and read out.

Next, the SEU robustness of this data cell is analyzed. Due to high symmetry of this circuit, the analysis can be simplified to the data “1” case. The data “0” case could resort to similar analysis. After the writing “1” process, the values at nodes Q1, Q1B, Q2, Q2B are “1”, “0”, “1”, “0”, and the values at nodes A, B, C, D are “0”, “1”, “0”, “1”, respectively. First, we shall find the sensitive nodes in this situation. Because the sensitive nodes of the integrated circuit are the surroundings of the reverse-biased drain junctions of a transistor biased in the OFF state [10], it is easily found out that nodes Q1, Q2B, C and D are sensitive nodes at the given initial “1” state in the data cell. The following discussion will make thorough explanation on the SEU robustness of each sensitive node.

Case 1-robustness of node Q1. Node Q1 is sensitive when the drain of the transistor N3 is struck by heavy ion. Q1 voltage tends to decrease after collection of excess charge induced by ion incidence. This temporarily shuts off N1 and N6, while turns on P5. Since Q1B remains Low, N4 keeps off. Q2 cannot be pulled down to ground, so it remains High. P1 keeps off and Q2B retains the original value.

Fig. 1. (a) Quatro-10T cell, (b) 18T cell, (c) 14T cell, (d) proposed cell.
Low. That is, the other nodes are not affected by the disturbance of node Q1, and they all keep their original values. Q1 eventually recovers to its original value High through the pull up path P3-N2.

**Case 2-robustness of node Q2B.** Node Q2B is sensitive when the drain of the transistor P1 is struck by heavy ion. Q2B voltage tends to increase after collection of excess charge induced by ion incidence. This temporarily shuts off P3 and P4, while turns on N5. Since Q2 remains High, P6 keeps off. Q1B cannot be pulled up to supply source, so it remains Low. N3 keeps off and Q1 retains the original value High. That is, the other nodes are not affected by the disturbance of node Q2B, and they all keep their original values. Q2B eventually recovers to its original value Low through the pull down path P2-N1.

**Case 3-robustness of node C.** Node C is sensitive when the drain of the transistor P6 is struck by heavy ion. C voltage tends to increase after collection of excess charge induced by ion incidence. Since transistor N5 is shut off, the transient voltage perturbation at node C cannot be propagated to other circuit nodes, thus the original circuit state is maintained.

**Case 4-robustness of node D.** Node D is sensitive when the drain of the transistor N4 is struck by heavy ion. D voltage tends to decrease after collection of excess charge induced by ion incidence. Since transistor P5 is shut off, the transient voltage perturbation at node D cannot be propagated to other circuit nodes, thus the original circuit state is maintained.

In the data “0” case, nodes Q1B, Q2, A and B are sensitive nodes, while nodes Q1, Q2B, C and D are inherently insensitive to ion strikes since the drains of surrounding transistors in OFF state are not reversely biased. The robustness of nodes Q1B, Q2, A and B in this case can be deduced by similar analysis.

### 3 Simulation results and discussion

The proposed SRAM data cell is implemented in 65 nm bulk CMOS process. Transistors P3, P6, N1 and N4 have significant impacts on the resilience of the circuit after ion hits, so they are sized a bit larger than the other transistors. It should be noted that larger transistor sizes are of benefit to the SEU robustness, while incur larger area overhead and power consumption. A compromise between the SEU tolerant capability and the performance cost should be carefully made according to the application requirements.

To simulate the injection of a particle and its associated charge deposition, an incoming (for the drain of OFF-state PMOS storing “0”) or outgoing (for the drain of OFF-state NMOS storing “1”) double exponential current pulse is usually connected to the sensitive node in Cadence Spectre as described below [6]

\[
I(t) = \frac{Q}{\tau_\alpha - \tau_\beta} \cdot (e^{-t/\tau_\alpha} - e^{-t/\tau_\beta})
\]

(1)

Where Q is the amount of charge deposited due to ion strike, \(\tau_\alpha\) is the collection time constant for the junction and \(\tau_\beta\) is the ion track establishment constant. According to [9], \(\tau_\alpha\) and \(\tau_\beta\) are set to 164 ps and 50 ps, respectively.

In the SPICE simulation, a logic “1” value is written into the data cell at the very beginning. After the circuit stabilizes, a double exponential current pulse is
injected into the sensitive nodes to mimic a particle-induced single event transient (SET). The writing signals and the injected SET current are shown in Fig. 2.

![Fig. 2. The inputs for writing logic “1” value and the injected double exponential current pulse for SET simulation.](image)

The writing process is initiated at 2.5 ns and finishes at 5.8 ns. At 20 ns, a double exponential current pulse ($I_{SET}$) with the peak value as high as 3.9 mA is injected into the sensitive nodes of the data cell to simulate a 1 pC particle-induced charge deposition. The transient responses of the storage nodes Q1, Q1B, Q2 and Q2B when $I_{SET}$ is injected into sensitive nodes Q1, Q2B, C and D are shown in Fig. 3∼Fig. 6, respectively.

![Fig. 3. Transient voltage responses of the storage nodes Q1, Q1B, Q2 and Q2B when $I_{SET}$ is injected into the sensitive node Q1.](image)

The initial written voltage of node Q1 is ~0.9 V, while node Q1B ~0 V at 1.2 V voltage supply. Although the stored values do not reach the full swing, the voltages are sufficient to represent logic High and logic Low. Simulation results suggest no flips occurring in the SRAM cell for all sensitive nodes. A 1 → 0 transient fault with voltage drop of 2.1 V (from 0.9 V to −1.2 V) is observed at node Q1 when the SET current hits node Q1. It takes about 2 ns for Q1 to recover to its original value High. Similarly, a 0 → 1 transient fault with voltage rise of 2.9 V (from 0.3 V to
3.2 V) is observed at node Q2B when the SET current hits node Q2B. It also takes about 2 ns for Q2B to recover to its original value Low. Almost negligible disturbances are incurred in the SRAM cell when the sensitive nodes C and D are hit by the SET current. SPICE simulations reveal superior SEU hardening capability of the proposed SRAM cell.
The performance of the proposed SRAM bit-cell is compared with the standard 6T cell, Quatro-10T cell, 18T cell and 14T cell. The comparison parameters include transistor number, critical charge, write time, power consumption, leakage current, power delay product (PDP) penalty and area penalty. The critical charge is obtained by the aforementioned current injection method, increasing the deposited charge amount until cell flip is observed. The write time is defined as the time interval between the midpoint of WL rising edge and the midpoint of storage node response edge. For fair comparison, the 18T cell which is originally designed in 0.18 µm standard digital CMOS technology is also implemented in 65 nm bulk CMOS technology, so that all data cells are compared at 65 nm technology node. Simulations of the proposed cell and the 18T cell are carried out with Cadence Spectre tool and 65 nm bulk CMOS models at 1.2 V voltage supply at room temperature with the working frequency of 100 MHz, while data for other cells under identical simulation conditions are obtained from published literature [5, 6]. The performance summary for comparative SEU hardened SRAM cells is shown in Table I. The PDP penalty and area penalty are given with reference to the standard 6T cell.

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<td>18</td>
<td>14</td>
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<td>25</td>
<td>95</td>
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<td>100%</td>
<td>174%</td>
<td>130%</td>
<td>140%</td>
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The proposed cell has an extremely large critical charge of 12320 fC, which is significantly greater than all the other designs, over 1000 times larger than that of the standard 6T cell. The write time is moderate compared to the others, and the leakage current is the lowest among all the hardened cells. The power consumption and hence the PDP penalty are a bit sacrificed, which might limit the low power applications of the proposed cell. The proposed cell occupies a relatively large area as the sensitive nodes are spaced out for charge sharing mitigation. Nevertheless, the area overhead is not too much and still less than the 18T cell. Overall, the proposed SRAM cell is excellent in SEU hardening capability and also electrical performances which guarantee high reliability in harsh radiation environment applications.

4 Conclusions

An improved SEU hardened SRAM bit-cell with differential read and write capability is proposed in this paper. An extremely high critical charge is achieved, over 1000 times larger than that of the standard 6T cell, which ensures high reliability of the proposed cell in harsh radiation environments. Meanwhile, the
proposed cell has comparable performances to previous SEU hardened designs, promising well-suited high performance applications.

Acknowledgments
This research is sponsored by the Foundation of Science and Technology on Analog Integrated Circuit Laboratory under contracts: 9140C090407150C09045 and 0C09YJTJ1601.