A 125–170 GHz wideband high-power amplifier using 0.5- μm InP DHBT

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Abstract: In this paper, a D-band power amplifier (PA) based on 0.5- μm InP DHBT is presented. Wilkinson combiners with broadband stepped-impedance matching are used, and the eight-way PA is designed for wideband power performance. As input power is fixed at 3 dBm, the PA exhibits a saturated output power of 16.8 dBm and 7.9% PAE at 150 GHz with >45-GHz 3-dB power bandwidth from 125 GHz to 170 GHz. Meanwhile the 1-dB gain compression output power is 15.9 dBm at 150 GHz. The >45-GHz 3-dB power bandwidth means a great flatness of power gain which is outstanding in reported D-band PAs to our best knowledge.

Keywords: D-band, InP DHBT, millimeter-wave, monolithic microwave integrated circuit (MMIC), wideband

Classification: Microwave and millimeter-wave devices, circuits, and modules

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1 Introduction

Recently, the upper millimeter-wave (100–300 GHz) integrated circuits (ICs) have attracted significant attention. Monolithic integrated power amplifiers (PAs) at this frequency range play a significant role in many applications [1, 2]. Among millimeter-wave band, D-band is especially promising for wireless communication due to the ISM band around 122 GHz and the atmospheric window with low free-space attenuation around 140 GHz. Recently, many D-band power amplifiers were reported utilizing Si/SiGe processes [3, 4, 5, 6].

Compared with Si/SiGe processes, InP HEMT and HBT technologies have obvious advantages in millimeter-wave and even higher frequency band due to their high $f_{\max}$ and better power capability. Lots of researches on InP HEMT and DHBT have been implemented these years, and many InP-based PAs aimed at the center frequency of 140 GHz [7, 8, 9, 10, 11] are reported. However, most of them mainly concentrate on higher output power, this may result in a poor flatness of power gain, which is significant for the practical bandwidth of transceiver in communication systems.

This paper presents the design of a 125–170 GHz wideband high-power amplifier using 0.5- μ m InP DHBT technology. The PA combines eight amplifier cells at the output stage using Wilkinson power combiners with broadband stepped-impedance matching instead of conventional quarter-wavelength transmission line for wideband performance. When the input power is fixed at 3 dBm, the PA achieves 16.8 dBm saturated output power with PAE of 7.9% at 150 GHz. Meanwhile a >45-GHz 3-dB power bandwidth with 31-GHz 1-dB power bandwidth, which is the widest power bandwidth reported for D-band monolithic integrated PAs to our best knowledge, is obtained.

2 Device process and characterization

The power amplifiers in this paper utilize a 0.5- μm InP DHBT process from Nanjing Electronic Devices Institute (NEDI) [12, 13]. The epitaxial layer of the DHBT was grown on 3-inch semi-insulating InP substrate using molecular-beam epitaxy (MBE). Good DC performance was obtained with a current gain (β) of around 33 and a common-emitter breakdown voltage (BV_{CEO}) of 4.8 V. When the transistor is biased at $V_C = 2$ V and $I_B = 550$ μA where the highest unity-gain cutoff frequency (f_T) and power-gain cutoff frequency (f_{max}) are obtained, the extracted f_T and f_{max} are 300 GHz and 400 GHz, respectively.

Besides the active device, passive circuits are implemented utilizing a three-metal-layer interconnect structure as illustrated in Fig. 1. The three metal layers (M1–M3) are separated by benzocyclobutene (BCB) with dielectric constant of 2.7. The thickness of M1 and M2 are both 1.5 μm and the top layer (M3) is 3 μm for a high-current capability. This fabrication technology also includes thin-film resistors (25 Ω/sq) on the device layer and metal-insulator-metal (MIM) capacitors (0.24 fF/ μm^2) with SiN_x between two capacitor metal layers. This work is performed on 620- μm full thickness InP substrate. In the future, the InP wafers will be thinned to 100- μm and populated with high-density backside-vias.

Fig. 1. Cross-section of the three-metal-layer InP DHBT process.

3 Design of the power amplifier

In order to realize high output power, we employ Wilkinson power combiners for input/output stage and inner stage combining. Conventional Wilkinson combiner, which contains two quarter-wavelength microstrip lines with 70.7- Ω characteristic impedance, is limited in bandwidth around the center frequency of the quarter-wavelength line and hard to be employed in this design because the quarter-wavelength at 140 GHz (330 μm) in this process is too short to accommodate eight amplifier cells. So broadband stepped-impedance matching is implemented instead of conventional quarter-wavelength transmission line in this design.

As for the amplifier cell, a two-stage cascaded CE topology is adopted. A modified Agilent-HBT model based on measurements is utilized for circuit design. The amplifier cell is designed for high output power across wide frequency band with input impedance of $(20-j \times 7.11) \Omega$ and output impedance of $(37.3-j \times 43.6) \Omega$, which are obtained from a load-pull simulation. The matching networks are thus

Fig. 2. Simulated S-parameters (a) and output power with input power swept from -5 to 1 dBm (b) of the amplifier cell.

designed to obtain a conjugate match of the input and output impedances over a wide bandwidth. The MIM capacitors and their parasitic effects are taken into consideration by EM simulation as a part of impedance matching network. The DC bias is fed through a transmission line shorter than a quarter wavelength which will expand the operating bandwidth and save space on the chip, thus the bias network is also included in the impedance matching network. Outside the feeding transmission line, RF signal is shorted by a 384 -fF grounded MIM capacitor and a 15 - Ω series resistor is utilized for low-frequency stabilization. Some compromises are made between high output power and wide power bandwidth in the matching networks. The transistor-access via-holes for leading signal from device layer onto M3 were also considered by EM simulation in the matching networks.

The simulated results of the amplifier cell are illustrated in Fig. 2(a) and (b). The amplifier cell exhibits a small signal gain of higher than 9 dB from 111 GHz to 162 GHz and return losses are better than 20 dB from 133 GHz to 153 GHz. The power simulation is also performed with input power swept from -5 to 1 dBm. When the input power is -1 dBm, the amplifier cell demonstrates higher than 7 dBm output power at 125 – 175 GHz, and the saturated output power is 8.1 dBm at 154 GHz. All of the results presented are simulated at the bias condition of $V_C = 2$ V and $V_B = 0.92$ V.

After the amplifier cell designing, power amplifier can be easily realized by combining several amplifier cells with power combiners in order to achieve higher

Fig. 3. Schematic (a) and microphotograph (b) of the eight-way PA.

output power. The schematic and microphotograph of proposed PA are presented in Fig. 3(a) and (b) respectively, which occupy $2\text{ mm} \times 1.9\text{ mm}$ without pads. The PA is constructed by cascading a four-way driving stage and an eight-way power stage for high output power, the driving stage and power stage are both based on the aforementioned two-stage amplifier cell.

4 Characterization of the PA

Both S-parameter measurement and power measurement of the PA IC are implemented on wafer. The S-parameter measurement of the D-band PA is carried out using an Agilent N5247A network analyzer with Farran 140–220 GHz frequency extender. LRRM on-wafer calibration is utilized to make sure the reference planes on the probe tips. The power performance is measured using a D-band power source and Erickson PM-4 powermeter. Due to the frequency limitation of Farran frequency extender in S-parameter measurements, we also use the power measurement setup to obtain small signal gain between 110 and 140 GHz with -15 dBm input power.

Fig. 4 shows the simulated and measured S-parameters at the bias condition of $V_C = 2\text{ V}$ and $I_B = 550\text{ }\mu\text{A}$. The PA exhibits higher than 15 dB small signal gain at 110–142 GHz and good return losses for both input and output ports. The measured power performances are depicted in Fig. 5. From Fig. 5(a) we can see the power gain with small input power agrees well with the S-parameter measurement. This PA delivers saturated output power of 16.5 dBm with PAE of 7.1% at 140 GHz, and

Fig. 4. Simulated (dashed) and measured (solid) S-parameters of the proposed PA.

Fig. 5. Measured power performance at 140 GHz (a) and measured power performance versus frequency with 3 dBm input power (b).

Table I. Comparison of reported D-Band PA ICs

Freq (GHz)	P _{sat} (dBm)	P _{1dB} (dBm)	PAE (%)	1-dB Power BW (GHz)	3-dB Power BW (GHz)	Technology	Reference
160	10	8.5	-	5	>9	130-nm SiGe	[4]
110–130	17.6	13.5	4.3	12	>20	120-nm SiGe	[5]
110–134	20.8	17	7.6	12	18	90-nm SiGe HBT	[6]
135–155	-	11.4	10.3	<8	>9	100-nm mHEMT	[9]
115–130	21.4	19	1.3	-	15	80-nm InP HEMT	[10]
125–170	16.8	15.9	7.9	>31	>45	0.5-μm InP DHBT	This work

the 1-dB gain compression output power is about 15.5 dBm which is 1 dB lower than the saturated output power due to the inherent high linearity of HBT. The amplifier consumes DC power of 590 mW at measured bias condition. Fig. 5(b) shows PAE and output power of the presented PA versus frequency with 3 dBm input power. A >45-GHz 3-dB output power bandwidth (i.e. power gain bandwidth) from 125 GHz to 170 GHz with 31-GHz 1-dB power bandwidth is obtained, and a peak output power of 16.8 dBm with PAE of 7.9% is achieved at 150 GHz.

Table I compares the reported monolithic integrated PAs operating at D-band. As we can see from the table, the presented work achieves competitive saturated output power and 1-dB gain compression output power. Great flatness of the power gain versus frequency is obtained with >45-GHz 3-dB power bandwidth from 125 GHz to 170 GHz and about 31-GHz 1-dB power bandwidth from 132 GHz to 163 GHz, this is the widest power bandwidth reported for D-band monolithic integrated PAs to our best knowledge.

5 Conclusion

In this paper, we report a monolithic integrated PA using 0.5-μm InP DHBT operating at D-band. The proposed PA combines eight amplifier cells at the last stage for higher output power. It exhibits a small signal gain of 15.2 dB at 140 GHz, a peak saturated output power of 16.8 dBm with PAE of 7.9%, a 1-dB gain compression output power of 15.9 dBm at 150 GHz, as well as wide output power bandwidth from 125 GHz to 170 GHz. The developed PA can be utilized in transceiver front ends and frequency multiplier chains at D-band. From this work, we can see a higher saturated output power will be easily realized by using 2-finger or 4-finger transistor, and next, the PA MMIC will be packaged after thinning the wafer to 100 μm and implementing backside-via process.