A D-band divide-by-6 injection-locked frequency divider with Lange-coupler feedback architecture in 0.13 µm SiGe HBT

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Abstract: A D-band divide-by-6 injection-locked frequency divider (ILFD) is presented. The basic mechanism of high division ratios frequency divider is investigated. The circuit employs a wideband microstrip Lange coupler, a microstrip delay line and a pair of Cascode transistors to form a feedback loop for enhanced divide-by-6 operation. The proposed ILFD is fabricated with chip size of 0.7 × 0.9 mm\textsuperscript{2} in a 0.13 µm SiGe HBT technology. The losses of WR-6 waveguide and 170-GHz probe in measurement setup are calibrated accurately by employing the open-short-load approach in a terminated two-port network. Through varying the operating voltage, the free-running oscillation frequency of the circuit can be changed, which results in an effective frequency-division locking range of 135 to 150.2 GHz while consuming 5.25 to 14.4 mW including the output buffer amplifier. A phase noise of $-121.58$ dBc/Hz at 1 MHz offset is achieved at 150.2 GHz.

Keywords: D-band, SiGe HBT, injection-lock, divider, Lange-coupler

Classification: Microwave and millimeter-wave devices, circuits, and modules

References


1 Introduction

The electromagnetic spectrum above 100 GHz has drawn a considerable amount of interest for imaging applications in medical, security, and non-destructive testing fields, as well as for military applications in target discrimination, air and space short range communications [1, 2]. The advances in silicon-based integrated circuits technologies have enabled implementation of millimeter-wave/terahertz systems using CMOS and BiCMOS technologies [3, 4], instead of III-V devices [5] which are limited by high cost and low integration level. No matter how the systems are defined, high-stability frequency sources are the heart, which makes frequency dividers play key roles in a typical phase-locked loop (PLL). However, the frequency dividers usually consume 75 percentage of the total power in mm-wave frequency synthesizer [6, 7, 8, 9]. The studies on frequency divider are performed in a number of publications to increase the maximum operation frequency and reduce the power consumption [10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22]. Generally, the high-speed frequency dividers can be classified into: Miller regenerative frequency divider [10, 11, 12, 13, 14], current-mode logic (CML) static frequency divider [15, 16] and injection-locked type [17, 18, 19, 20, 21, 22]. Regenerative frequency dividers are widely used in high frequency and wide bandwidth applications. They are fundamentally a non-linear feedback loop consisting of a mixer and a low-pass filter. Unfortunately, extreme high power dissipation is a serious drawback in low-power systems. Theoretically, regenerative frequency dividers are able to achieve the arbitrary division ratio. However, the circuit topology will get more complex, as well as the power consumption higher, due to the introducing of the frequency multiplication sub-circuit in feedback loop. A static frequency divider usually realized with CML, as depicted in [14], is an interesting alternative for millimeter-wave applications through semiconductor technology scaling. Similarly, the power consumption enormously increases with the increasing of the operation frequency. Injection-locked frequency divider (ILFD) is a good candidate for millimeter-wave and low-power applications. Conventional LC-based ILFD easily realizes the highest operation frequency, compact circuit size and low dc power consumption [18], while its locking range is usually limited by the high Q nature. The reported frequency dividers whose division ratios are better than two are primarily based on ring-oscillator topology [23, 24]. But the operation speed of ring-oscillator-based ILFD is inferior to the LC cross-coupled type. Within a given input frequency, the free-running oscillation frequency and power requirement of the ILFDs can be reduced through increasing...
the division ratio. And the requirements for the subsequent frequency-divider stages in mm-wave frequency synthesis applications are released.

Consequently, it is fascinating to find out a solution to simultaneously satisfy high operation frequency, high division ratio, low power consumption, acceptable locking range, and sufficient power output capability. Though the Lange coupler has been put forward for over 40 years and is quite useful in the design of the balanced amplifier, various mixers and balanced doublers, the Lange coupler is seldom used in frequency divider. In this paper, a feedback technique is presented for the design of a divide-by-6 ILFD. A microstrip Lange coupler, a microstrip delay line and a pair of Cascode transistors to form a feedback loop is introduced to increase the injection efficiency and reduce power consumption.

The paper is organized as follows. Section II describes the operation mechanism of divide-by-6 ILFD. The topology of frequency divider and circuit implementation are presented in Section III, the correction method of waveguide loss and measurement results is shown in Section IV. And finally, the paper is summarized in Section V.

2 Operation mechanism of divide-by-6 ILFD

As depicted in Fig. 1 [23], the injection-locked frequency divider works by synchronizing an oscillator with an incident signal. In this model, $v_i(t)$ is defined as the injected signal, $v_o(t)$ is the output signal, $f(e)$ is the nonlinear multiplication of incident signal and feedback signal, the $H(\omega)$ is the frequency selection network. If external signal is not injected, the circuit acts as a free-running oscillator. When an additional signal is injected from the outside of the loop, if the amplitude and frequency of the injected signal are properly chosen, the phase shift contributed by the nonlinearity $f(e)$ will be changed to compensate the phase shift introduced by the injected signal, the circuit oscillates at a new frequency, and injection locking occurs at the input frequency $\omega_i$ itself, or a subharmonic or superharmonic of $\omega_i$. Then the original oscillation frequency of the loop will get disappeared. In [23], the conditions for divide-by-2 ILFD are derived. But what will happen for a divide-by-6 application?

![General model of a injection-locked oscillator](image)

For frequency dividers, the output signal $v_o$ can be written as,

$$v_o(t) = V_o e^{i\omega_o t} = \frac{H_{0e} e^{i\omega_i t}}{1 + j2Q\frac{\Delta \omega}{\omega_o}} \left[ K_{0,1} + \frac{1}{2} \sum_{m=1}^{\infty} K_{m,1} e^{im\theta} \right]$$

(1)
The real and imaginary part of (1) can be separated, and the fundamental equations for injection-locked frequency divider can be obtained.

\[ V_o = H_0 \left[ K_{0,1} + \frac{1}{2} \sum_{m=1}^{\infty} K_{m,n} \cos(m\theta) \right] \]  
(2)

\[ 2V_o \frac{\Delta \omega}{\omega_r} = \frac{H_0}{2} \sum_{m=1}^{\infty} K_{m,n} \sin(m\theta) \]  
(3)

where \( \omega_r \) and \( Q \) are the resonant frequency and quality factor, respectively. \( \Delta \omega \) is the offset frequency. \( \theta \) is the phase difference between the input and output signal.

For the case of \( N = 6 \) and \( f(e(t)) \) can be expressed by a seventh-order nonlinear equation,

\[ f(e(t)) = a_0 + a_1 e + a_2 e^2 + a_3 e^3 + a_4 e^4 + a_5 e^5 + a_6 e^6 + a_7 e^7 \]  
(4)

The phase condition can be obtained by solving the equation (3),

\[ \sin \theta = \frac{32Q}{3H_0 a_6 V_i V_o^4} \frac{\Delta \omega}{\omega_r} \]  
(5)

with \( | \sin \theta | < 1 \), then,

\[ \left| \frac{\Delta \omega}{\omega_r} \right| < \left| \frac{3H_0 a_6 V_i V_o^4}{32Q} \right| \]  
(6)

As (6) suggested, the locking range can be increased by either raising \( H_0/Q \) or the injected signal amplitude \( V_i \). Meanwhile, from (6), there is an additional requirement for the output signal amplitude of divide-by-6 ILFD. If the result does not satisfy the condition of (6), the loop will fail to lock. Moreover, \( a_6 \) is the sixth harmonic coefficient which require large bandwidth to cover the whole band from \( \omega_r \) to \( 6\omega_r \).

On the other hand, the gain condition can be solved by (2),

\[ \frac{5}{8} a_7 V_o^6 + \left( \frac{5}{8} a_5 + \frac{105}{8} a_7 V_i^2 + \frac{3}{16} a_6 V_i \cos \theta \right) V_o^4 \]

\[ + \left( \frac{3}{4} a_3 + \frac{15}{2} a_5 V_i^2 + \frac{315}{16} a_7 V_i^4 \right) V_o^2 \]

\[ + \left( 2a_1 + 3a_3 V_i^2 + \frac{15}{4} a_5 V_i^4 + \frac{35}{8} a_7 V_i^6 - \frac{1}{H_0} \right) = 0 \]  
(7)

If the equation (7) is not satisfied, the injection locking also fails. As a result, the high-order injection locking is determined by both the phase and gain conditions.

3 Circuit design and simulation

Fig. 2 shows the circuit schematic of the proposed HBT ILFD. The core circuit consists of a cascode transistor pair (T1 and T2), a microstrip Lange coupler, phase compensation block (ML2) and a buffer amplifier with impedance matching networks.

Based on the conclusion from (6), a wideband coupler is desired to achieve six division, in order to obtain small enough loss at the frequency of input signal and
the one-sixth harmonic, respectively. The conventional Lange coupler [25], as depicted in Fig. 3, is widely used for power distribution or combination with 90° phase shift in various microwave/mm-wave integrated circuits. It has the advantages of the amplitude balance, high isolation between the coupled port 3 and through port 2, and inherent wideband characteristics. In this design, its features are used to form a feedback oscillator and excellent coupled output structure. The design of Lange coupler is exhibited to find an optimal spacing gap and line width according to the expected 3-dB coupling coefficient and process requirements based on odd- and even-mode impedance theory [26]. The odd-mode impedance is defined as,

$$Z_{0o} = Z_0 \left( \frac{1 - c}{1 + c} \right)^{1/2} \frac{(N - 1)(1 + q)}{(c + q) + (N - 1)(1 - c)}$$  \hspace{1cm} (8)$$

where, $N$ is the even number of fingers, $c$ is the voltage coupling coefficient, defined as,

$$c = \frac{(N - 1)(1 - R^2)}{(N - 1)(1 + R^2) + 2R}$$  \hspace{1cm} (9)$$

coefficient $q$ can be obtained from (10),

![Fig. 2. The schematic of the Lange-coupler based ILFD](image)

![Fig. 3. Top view and cross-section view of the conventional Lange coupler](image)
\[ q = \left[ c^2 - (c^2 - 1)(N - 1)^2 \right]^{1/2} \]  

(10)

R is the impedance ratio, which can be got as following,

\[ R = \frac{Z_0o}{Z_0e} \]  

(11)

equation (9) can be solved for R,

\[ R = \frac{\sqrt{c^2 - (c^2 - 1)(N - 1)^2} - c}{(c + 1)(N - 1)} \]  

(12)

Then the even-mode impedance \( Z_{0e} \) can be solved by substituting (11) into (9). Based on the equations mentioned above and the process design rule, the optimum spacing gap and line width can be obtained. The isolated port is terminated by a 50 \( \Omega \) resistor. The Lange coupler is bent in the form of a polygon to reduce the chip size, whose layout and simulated frequency response are shown in Fig. 4. The central frequency of the Lange coupler lies around the 1/6 of the 140 GHz, and the special shape does not induce very high loss.

The cascode transistors formed by T1 and T2 which are conventionally used for solving the Miller effect can provide higher loop gain and wider gain bandwidth, and is able to compensate the losses of the Lange coupler and feedback path so as to make the closed loop maintain the positive feedback with the phase compensation of delay line ML2. The cascode topology is a combination of a common-emitter and common-base HBTs, as depicted in Fig. 2. It can reduce the effect of the feedback capacitance (\( C_{bc} \)) in common-emitter HBT and widen the gain bandwidth. The mm-wave signal is injected to the base of the common-base transistor T1, and the feedback signal is added to the base of the common-emitter transistor T2. Through tracking the phase of the injected signal, if the phase condition is satisfied, the output frequency will be locked at the 6th-order super-harmonic of the input frequency. The locked signal is extracted from the coupled port \( P_3 \) of the Lange coupler and provided to the output buffer T3. Therefore, the peripheral circuits do not have significant effect on the core oscillator due to the high isolation feature between the two ports. A buffer stage T3 is used to provide high impedance load for core divider circuit and maximize the output power level, which will result in a wider and stable locking range. It is consistent with the conclusion of eq. (6).

**Fig. 4.** Layout and simulated frequency response of bended Lange coupler
4 Experimental results

The proposed injection-locked frequency divider circuit has been fabricated in the 0.13 µm SiGe HBT technology with $f_T = 240$ GHz and $f_{MAX} = 330$ GHz. The chip photograph is shown in Fig. 5, and the circuit occupies $0.7 \times 0.9$ mm² chip area.

![Microphotograph of the fabricated frequency divider](image)

**Fig. 5.** Microphotograph of the fabricated frequency divider

The measurement setup is shown in Fig. 6. The equipments of on-wafer measurement consist of signal generator, spectrum analyzer, D-band multiplier module, and several connection components. The input power is calibrated by a millimeter-wave power meter. The output power of the multiplier module is limited around 4 dBm at the frequency range from 135~150 GHz. A great deal of uncertainty introduced by unknown loss of the waveguide and D-band waveguide probe at such high operation frequency band is difficult to be characterized. Usually, the loss is roughly predicted in experiments. However, the entire loss characteristic of the connected WR-6 waveguide and D-band probe is important for the measurement to obtain accurate input power level at the end of the probe tip.

![Measurement setup](image)

**Fig. 6.** Measurement setup

Considering a terminated two-port network [26] depicted in Fig. 7. The nodes $a_1$, $a_2$, $b_1$, $b_2$ are defined as,

\[ b_1 = a_1 S_{11} + a_2 S_{12} \]  \hspace{1cm} (13)
\[ b_2 = a_1 S_{21} + a_2 S_{22} \]  \hspace{1cm} (14)

$\Gamma_{in}$ is given by the ratio of $b_1/a_1$, when the network is terminated by $Z_L$, $a_2 \neq 0$ and

\[ a_2 = b_2\Gamma_L = (a_1 S_{21} + a_2 S_{22})\Gamma_L \]  \hspace{1cm} (15)

where \[ \frac{a_2}{a_1} = \frac{S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \]

Then $\Gamma_{in}$ is solved by,
In above equation, there are four unknown parameters. The simplest way to solve it is to use three or more known loads, such as open, short and matched load. Therefore, the unknown parameters are solved by,

\[ S_{11} = \Gamma_{in, \text{load}} \]  \hspace{1cm} \text{(17)}

\[ S_{22} = \frac{2S_{11} - \Gamma_{in, \text{short}} - \Gamma_{in, \text{open}}}{\Gamma_{in, \text{short}} - \Gamma_{in, \text{open}}} \]  \hspace{1cm} \text{(18)}

\[ S_{12}S_{21} = \frac{(\Gamma_{in, \text{open}} - \Gamma_{in, \text{short}})(1 - S_{22}^2)}{2} \]  \hspace{1cm} \text{(19)}

Since the actual under-test network combined the waveguide and probe is not a symmetrical network, however, the equation (19) will be unsolvable. Setting \( S_{21} = S_{12} \), that equation belongs to a complex root problem. According to the DeMoivre’s theorem, the two-port network is obtained with this approach, as shown in Fig. 8.

There is a free-running oscillation phenomenon while no input signal injects. The measured free-running oscillation frequency of the ILFD varies from 22.83 to 24.9 GHz while consuming 5-to-9 mA current including the buffer amplifier at 1.05-to-1.6 V power supply, as shown in Fig. 9.

The measured input sensitivity curves of the ILFD under different voltage are shown in Fig. 10. Operated with a 1.05 V dc supply consuming 5 mA current and around 2 dBm input signal, the divider exhibits a locking range of 2.77% from 135
to 138.8 GHz. As the supply voltage is increased to 1.6 V, the maximum operation frequency is extended up to 150.2 GHz with a power dissipation of 14.4 mW.

Fig. 9. Free-running oscillation frequency variation by sweeping the bias voltage $V_{cc}$

Fig. 10. Measured input sensitivity of the ILFD under different supply voltage

Fig. 11. Measured output spectrum and phase noise with the input signal frequency of 135 GHz and $V_{cc} = 1.05$ V consuming 5 mA current shown in (a) and (b)

Fig. 11 and 12 show the measured spectrum under the input frequency of 135 GHz and 150.2 GHz, respectively. A −5.69 dBm output is obtained before the cable loss is calibrated, at the operation frequency of 150.2 GHz. Phase noise measurement results shown in Fig. 11(b) and Fig. 12(b) indicate around −121 dBC/Hz at 1 MHz offset for the operation frequency of 135 GHz and 150.2 GHz, respectively. They are limited by the input source phase noise of
−106 dBc/Hz at 1 MHz offset. The improved phase noise of 15 dB obeys the rule of $20 \log N$.

The ILFD performance summary and comparison with the reported state-of-the-art ILFDs are presented in Table I. Compared with the reported frequency dividers with highest operation frequency, the proposed ILFD can operate at millimeter-wave band while achieving divide-by-6 function and maintaining high power output level to drive next-stage frequency divider in PLL.

**Table I.** Performance summary and comparison

<table>
<thead>
<tr>
<th></th>
<th>[18]</th>
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<td>Technology</td>
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<td>65 nm</td>
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<td>0.13 µm SiGe HBT</td>
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<tr>
<td>Type</td>
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<td>Injection-locked</td>
<td>Injection-locked</td>
<td>Miller</td>
<td>Injection-locked</td>
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<tr>
<td>Locking range (GHz)</td>
<td>181 to 208</td>
<td>198.9 to 201</td>
<td>128.24 to 137</td>
<td>51 to 168</td>
<td>135 to 150.2</td>
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<tr>
<td>Division ratio</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>6</td>
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<tr>
<td>Phase noise</td>
<td>−91.6 dBc/Hz @100 KHz</td>
<td>−78.81 dBc/Hz @400 KHz</td>
<td>−121.58 dBc/Hz @1 MHz</td>
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<tr>
<td>Input power (dBm)</td>
<td>−1</td>
<td>−4</td>
<td>−4</td>
<td>−4</td>
<td>2</td>
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<td>&quot;Output power (dBm)</td>
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<td>−18.47</td>
<td>−</td>
<td>−</td>
<td>−5.69</td>
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<td>Supply (V)</td>
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<td>1.1</td>
<td>4</td>
<td>1.05~1.6</td>
</tr>
<tr>
<td>Power diss. (mW)</td>
<td>2.4</td>
<td>8.8</td>
<td>5.5</td>
<td>105</td>
<td><strong>5.25 to 14.4</strong></td>
</tr>
<tr>
<td>Chip area (mm²)</td>
<td>0.12 × 0.09</td>
<td>0.2 × 0.16</td>
<td>0.32 × 0.16</td>
<td>***0.58 × 0.4 8</td>
<td>***0.7 × 0.9</td>
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*The output power is not calibrated
**Including the output buffer amplifier
***Overall chip area
5 Conclusion

The analysis, design and measurement of a new injection-locked frequency divider (ILFD) are presented in this paper. It has the function of divide-by-6. Through changing the free-running oscillation frequency of the core circuit by sweeping the supply voltage, the fabricated ILFD is able to cover the locking range of 135 GHz to 150.2 GHz while consuming 5.25 to 14.4 mW including the buffer amplifier. The experimental results show that this solution can simultaneously satisfy high operation frequency, high division ratio, low power consumption, acceptable locking range, and sufficient power output capability.