A radiation harden enhanced Quatro (RHEQ) SRAM cell

Chunyu Peng^{1a)}, Ziyang Chen¹, Jingbo Zhang^{1,2}, Songsong Xiao¹, Changyong Liu¹, Xiulong Wu^{1b)}, and Zhiting Lin^{1c)}

¹ School of Electronics and Information Engineering, Anhui University, Hefei 230601, China

² Industry Development and Promotion Center, Ministry of Industry and Information Technology of the Peoples Republic China, Beijing 100804, China

a) cyupeng@ahu.edu.cn

b) xiulong@ahu.edu.cn, Corresponding Author

c) ztlin@ahu.edu.cn, Corresponding Author

Abstract: This paper intends to present a novel radiation-hardened SRAM cell by using the PMOS transistors stacked (each PMOS is split into two same sizes) and changing the inner topological structure on basis of the Quatro-10T. Combined with layout-level optimization design, the 3-D TCAD mixed-mode simulation results show that the novel design has a great single event upset (SEU) immune. Simultaneously, it is found to be tolerant of partial single-event multiple-node upsets (SEMNUs) due to the charge sharing among off-PMOS transistors. In addition, compared with the Quatro-10T, our proposed structure exhibits larger static noise margin (SNM) as well as lower power consumption in 65 nm COMS technology.

Keywords: radiation-hardened SRAM, single event upset, single-event multiple-node upsets, static noise margin, lower power consumption

Classification: Integrated circuits

References

- [1] E. Ibe, *et al.*: “Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule,” *IEEE Trans. Electron Devices* **57** (2010) 1527 (DOI: [10.1109/TED.2010.2047907](https://doi.org/10.1109/TED.2010.2047907)).
- [2] P. E. Dodd and L. W. Massengill: “Basic mechanisms and modeling of single-event upset in digital microelectronics,” *IEEE Trans. Nucl. Sci.* **50** (2003) 583 (DOI: [10.1109/TNS.2003.813129](https://doi.org/10.1109/TNS.2003.813129)).
- [3] C. Qi, *et al.*: “A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets,” *IEEE Trans. Device Mater. Rel.* **16** (2016) 388 (DOI: [10.1109/TDMR.2016.2593590](https://doi.org/10.1109/TDMR.2016.2593590)).
- [4] S. M. Jahinuzzaman, *et al.*: “A soft error tolerant 10T SRAM bit-cell with differential read capability,” *IEEE Trans. Nucl. Sci.* **56** (2009) 3768 (DOI: [10.1109/TNS.2009.2032090](https://doi.org/10.1109/TNS.2009.2032090)).
- [5] T. Calin, *et al.*: “Upset hardened memory design for submicron CMOS technology,” *IEEE Trans. Nucl. Sci.* **43** (1996) 2874 (DOI: [10.1109/23.556880](https://doi.org/10.1109/23.556880)).
- [6] H.-B. Wang, *et al.*: “An area efficient SEU-tolerant latch design,” *IEEE Trans. Nucl. Sci.* **61** (2014) 3660 (DOI: [10.1109/TNS.2014.2361514](https://doi.org/10.1109/TNS.2014.2361514)).
- [7] H.-B. Wang, *et al.*: “An area efficient stacked latch design tolerant to SEU in

- 28 nm FDSOI technology,” IEEE Trans. Nucl. Sci. **63** (2016) 3003 (DOI: [10.1109/TNS.2016.2627003](https://doi.org/10.1109/TNS.2016.2627003)).
- [8] S. Jagannathan, *et al.*: “Single-event tolerant flip-flop design in 40-nm bulk CMOS technology,” IEEE Trans. Nucl. Sci. **58** (2011) 3033 (DOI: [10.1109/TNS.2011.2170201](https://doi.org/10.1109/TNS.2011.2170201)).
- [9] Q. Wu, *et al.*: “Supply voltage dependence of heavy ion induced SEEs on 65 nm CMOS bulk SRAMs,” IEEE Trans. Nucl. Sci. **62** (2015) 1898 (DOI: [10.1109/TNS.2015.2454954](https://doi.org/10.1109/TNS.2015.2454954)).
- [10] L. D. T. Dang, *et al.*: “Studying the variation effects of radiation hardened Quatro SRAM bit-cell,” IEEE Trans. Nucl. Sci. **63** (2016) 2399 (DOI: [10.1109/TNS.2016.2590426](https://doi.org/10.1109/TNS.2016.2590426)).
- [11] J. Chen, *et al.*: “Radiation hardened by design techniques to reduce single event transient pulse width based on the physical mechanism,” Microelectron. Reliab. **52** (2012) 1227 (DOI: [10.1016/j.microrel.2011.12.002](https://doi.org/10.1016/j.microrel.2011.12.002)).
- [12] J. Chen, *et al.*: “Simulation study of the layout technique for P-hit single-event transient mitigation via the source isolation,” IEEE Trans. Device Mater. Rel. **12** (2012) 501 (DOI: [10.1109/TDMR.2012.2191971](https://doi.org/10.1109/TDMR.2012.2191971)).
- [13] Y. Du, *et al.*: “A constrained layout placement approach to enhance pulse quenching effect in large combinational circuits,” IEEE Trans. Device Mater. Rel. **14** (2014) 268 (DOI: [10.1109/TDMR.2013.2291409](https://doi.org/10.1109/TDMR.2013.2291409)).
- [14] O. A. Amusan, *et al.*: “Single event upsets in deep-submicrometer technologies due to charge sharing,” IEEE Trans. Device Mater. Rel. **8** (2008) 582 (DOI: [10.1109/TDMR.2008.2000892](https://doi.org/10.1109/TDMR.2008.2000892)).
- [15] J. R. Ahlbin, *et al.*: “Effect of multiple-transistor charge collection on single-event transient pulse widths,” IEEE Trans. Device Mater. Rel. **11** (2011) 401 (DOI: [10.1109/TDMR.2011.2157506](https://doi.org/10.1109/TDMR.2011.2157506)).
- [16] J. R. Ahlbin, *et al.*: “Double-pulse-single-event transients in combinational logic,” Proc. IEEE IRPS (2011) 258.

1 Introduction

With the continuous advancement in the field of integrated circuits (ICs) technology, the density of chip integration has greatly improved. Circuits have become more sensitive to radiation making the reliability issue to become one of the major concerns of circuit designs [1]. For circuits operating in space radiation environments, semi-conductor material struck by high-energy particles, electrons as well as holes are generated along the penetration path. These surplus carriers might be gathered by the sensitive nodes through drift and diffusion as a consequence, resulting in a current (also known as voltage) perturbation at that node [2]. For memory cell, when the amplitude of the voltage perturbation is strong enough, the data stored might be altered temporarily, which may result in a SEU [3]. Moreover, with technology scaling, circuit nodal capacitances and supply voltage has been reduced radically, which makes static random access memory (SRAM) more vulnerable to SEU. For SEU tolerable design, two types of hardened cell Quatro-10T [4] and DICE [5], as memory or latch or flip-flop cell, are broadly studied owing to their good SEU immunes [4, 5, 6, 7, 8]. DICE majorly relies on the extra principle of dual node feedback control to make it fully immune against a single node upset. However, this cell has very minimal ability of single-event multiple-node upsets (SEMNUs) immune. In Quatro-10T cell, each node is connected to the

gate of two PFET (NFET) devices. A SET on single node might turn on both devices simultaneously and then flip the cell. Thus, Quatro-10T is not fully immune to single node upset. For Quatro-10T as well as DICE cells, one does not constantly demonstrate superior hardening performance over the other [9]. Nevertheless, as an alternative to DICE, Quatro-10T has been shown to be more powerful and area efficient [4]. On the other hand, it displays larger noise margin in sub-0.4V regime with less leakage current than DICE cell. Therefore, the application of it is extremely promising in the radiation environment. However, the read and write (R/W) mechanisms of Quatro-10T are incredibly similar to those of 6T SRAM cell. This means that it might suffer from weak R/W stabilities under process and temperature variations, when technology size scales continuously. To enhance the write stability of Quatro-10T, [10] obtained write operation frequency up to 250 MHz by employing the boosted voltage of word-line and bit-line at the worst process and temperature condition.

In this paper, a radiation harden enhanced Quatro (RHEQ) SRAM cell is proposed. It enhances the write margin (WM) as well as read margin (RM) by changing inner topological structure and employing R/W separation. Unlike original Quatro-10T, each PMOS in the proposed RHEQ cell is split into two same size transistors stacked together. Combined with the layout-level design, the simulation results show that the novel design has better SEU immune than the Quatro-10T.

2 Proposed circuit

Fig. 1. Schematic and sizing of (a) Quatro-10T and (b) proposed SRAM cell (width and length units are nm).

The hardening technique by stacked transistor has been demonstrated according to the reference [7, 11]. Thus, on the basis of original Quatro-10T cell in Fig. 1(a), it divides the PMOS (PC and PD) into two same sizes of PMOS (Pc1 and Pc2, as well as Pd1 and Pd2) in the proposed RHEQ SRAM cell illustrated in Fig. 1(b). Meanwhile, the PMOS (PA and PB) are also divided into two same sizes of PMOS (Pa1 and Pa2, as well as Pb1 and Pb2), after that the inner topological structure is

changed in order to achieve the high write margin (WM). Moreover, the access transistors AL (AR) are further divided into two same sizes of AL1 as well as AL2 (AR1 and AR2), and the NMOS drive transistors (NL1, NL2, NR1, and NR2) still remain. As a result, the area of the proposed RHEQ is almost same as that of the Quatro-10T owing to the dividing method, and the sizes of the transistor for the both cell are shown as Fig. 1. Additionally, the storage nodes are Q and QB, which are connected to BL and BLB through the access transistor AL1 as well as AR1, respectively. Redundant nodes X0 and X1 are connected to BLB and BL via access transistor AR2 and AL2, respectively.

Fig. 2. The inner signals of the proposed RHEQ cell with Q = '0'.

The proposed structure employed the WWL and RWL as the write and read word line, respectively. In write operation, the selected RWL and WWL are set to 0 and VDD, respectively. We first presume that the potential of Q, QB, X0 and X1 are '0', '1', '1', and '0', respectively (as shown in Fig. 2). The BL is set to VDD, while the BLB is set to 0. Node QB will pull-down by BLB whereas node Q will pull-up by BL. In read operation, BL and BLB are pulled up to high potential by the pre-charge circuit block. The selected RWL and WWL are set to VDD and 0, respectively. Node QB and X0 keep the initial value of '1', whereas BL will discharge to 0 through AL2 and NR2. When the differential voltage between BL and BLB is established, a read operation is performed and the data of the memory cell is output by the sense amplifier.

Compared with the Quatro-10T, the proposed structure has greatly improved in WM as well as RM by adopting R/W separation. Additionally, due to the sources of Pa2 and Pb2 are connected with the drain of Pa1 and Pb1, respectively, rather than the VDD. The leakage current and write time decreased significantly. These conclusions will be verified in the next section.

In the circuit-level, for analyzing the SEU toleration efficiency of the proposed cell, referring to Fig. 2, we assume that Q = '0', QB = '1', X0 = '1', X1 = '0', WWL = '0', and RWL = '0', respectively. Correspondingly, the vulnerabilities of the nodes (Q, QB, X0, and X1) are demonstrated as follow.

Case1-vulnerability of node Q: for the X0 = '1', hence, Pc1, Pc2, Pb1, and Pb2 keep the off state, when the drain of Pc1 is struck, it will collect charge (hole) and

cause the potential of Q arise, consequently NL2 and NR1 are turned on. The potential of X0 together with QB will go down. Accordingly, Pb1 will turn on while NR2 will be turned off. Thus, the storage value will also be turned over ultimately (it has been made difficult to change to '1' in the layout level design as shown in the next section). Compared with the Quatro-10T cell, due to the transistors stacked and topology optimized, the parasitic bipolar amplification effect of Pc1 (the source of PC is connected with VDD, whereas the source of Pc1 is connected with weak '1') is mitigated. As a result, the quantity of charge collected by Pc1 drain is reduced, which improves the SEU tolerance of node Q.

Case2-vulnerability of node QB: for the $Q = '0'$, the NR1 is off. When the drain of NR1 is struck, it will collect charge (electron) and result in the potential of QB declining which just makes the NL1 and NR2 turn off. Meanwhile, due to the node $X1 = '0'$, the Pa1 will still remains on, thus, the potential of node X0 is hardly declined. As the result, the potential of QB will recover to '1' in the end.

Case3-vulnerability of node X0: for the $Q = '0'$, the NL2 is off. When the drain of NL2 is struck, it will collect charge (electron) and cause the potential of X0 to decline. The Pb1 will be turned on, whereas the QB will remain the weak '1' due to the feedback control mechanism of the circuit. Meanwhile, the size of Pb1 will be smaller than NR2, thus, the potential of X1 will be hard to rise. As a result, the potential of X0 will recover to '1' by Pa1 at last.

Fig. 3. Layouts of (a) the proposed RHEQ and (b) Quatro-10T.

Case4-vulnerability of node X1: for the $X0 = '1'$, the Pb1 is off. When the drain of Pb1 is struck, it will collect charge (hole) and cause the potential of node X1 to rise, as a result, PMOSs (Pa1, Pa2, Pd1 and Pd2) are turned off. However, this change cannot further affect the off/on states of other transistors. Node QB will remain the logic value of '1', while the NR2 will also still remain at the on state. The potential of X1 will recover to '0' by NR2 in the end.

Based on the above circuit-level analyses, we can find out that the node Q (or QB depending on store state) is the weakest node. At the layout-level design, therefore, it is crucial for us to make it stronger. As illustrated in Fig. 1(a), the drains of the off-transistors are the sensitive areas. When the drain of PC (off-state) is struck, lots of holes will be injected into the N-well from the VDD due to the bipolar effect. Consequently, the number of holes collected by the drain is increased. Therefore, mitigating the bipolar effect in the PMOS connected the storage node is prior selection for enhanced the SRAM SEU immune. The source isolation

technique was presented in [11] and [12], which has been found that it can mitigate P-hit single-event transient perceptibly. Thus, based on the source isolation, the special design of stacking PMOS transistors with layout-level optimized is beneficial for the proposed cell to mitigate the upset from ‘0’ to ‘1’ (occurring on node Q). In case 1, when the drain of Pc1 is struck, the NR1 and NL2 are affected. This will foster the upset of SRAM cell. Therefore, we make the off-transistor NR1 together with NL2 distant from the other off-PMOS transistors so as to avoid charge sharing between them. The layout of the proposed RHEQ cell is illustrated in Fig. 3(a). It is observable that the drain (the charge collection region) of Pc1 (Pd1) is directly isolated from Pb1 (Pa1) (the hole injection region) by STI and Pb2. Additionally, since the potential of Pb2 source is 0, during the hold state, the source potential of Pc2 becomes weak ‘1’ rather than the prior VDD. Thus, it makes the Pc1 (Pd1) drain to collect charge (hole) hardly, when it suffers from ion striking.

From all the circuit-levels and layout-levels optimized above, the node Q of our proposed memory cell can be as strong as possible. This deduction will be proven through the TCAD mixed-mode simulation in the next section.

3 Simulation results and analysis

In this section, the circuit-level simulation results will be provided. All of the following simulations use 65 nm commercial technology with 1.2 V power supply at 27°C.

Table I. Performance comparisons between the RHEQ and Quatro-10T at TT, 1.2 V, and 27°C

	Read time/ns	Write time/ns	Read current / μ A	Write current / μ A	Leakage current /nA	Dynamic power / μ W
Quatro-10T	0.104 (100%)	1.754 (100%)	1.115 (100%)	65.68 (100%)	0.18 (100%)	40.08 (100%)
Proposed RHEQ	0.149 (143%)	0.969 (55%)	0.52 (47%)	15.43 (24%)	0.157 (83%)	9.57 (24%)

Fig. 4. The waveform of the proposed RHEQ as well as Quatro-10T.

Fig. 4 illustrates the timing of the proposed RHEQ and Quatro-10T, as shown, it can deduce that the write time of the proposed cell is reduced by 0.785 ns compared with the Quatro-10T. Moreover, the performance comparisons between the RHEQ and Quatro-10T at TT, 1.2 V, and 27°C are summarized in Table I, in

which the read access time is measured when there is a 200 mV differential voltage between the two bit lines. As presented, the proposed RHEQ has clearly brought down the leakage current and dynamic power consumption. And the read delay can further be optimized by adjusting the size of AL2 as well as AR2, which is observed to have no effect on other performances.

In order to present the high reliability of the proposed RHEQ, Fig. 5 and Fig. 6 give the RM and WM comparison between it and the original Quatro-10T under different process corners and voltages, respectively. As shown, the proposed cell has great improvement of both read and write margin.

Fig. 5. RM and WM comparison between the proposed RHEQ and Quatro-10T under different process corners.

Fig. 6. RM and WM comparison with varying voltages at TT corner and 25 °C.

For investigating single-event effects in ICs, the three-dimensional mixed-mode (TCAD) simulation has been confirmed to be a practical means [3, 13, 14, 15]. Thus, with using the Sentaurus TCAD, the TCAD models in this paper are calibrated from commercial 65 nm bulk CMOS process design kit (PDK) to make sure that the electrical characteristics between them are matched well. And, the

calibration results of the Id-Vd and Id-Vg currents are shown as Fig. 7. Here, the transistors are made on the P-substrate with a constant doping of $1 \times 10^{16} \text{ cm}^{-3}$. And the buried P+ deep well is implanted with the Gaussian doping profile whose peak value is $1 \times 10^{18} \text{ cm}^{-3}$. Moreover, the back side of substrate contact is utilized along the bottom surface. The TCAD heavy ion physical model as the striking ion is employed with the charge track length and radius fixed at 10 μm and 50 nm, respectively. Additionally, the ion striking at the center of the drain of the struck device, as well as the LET value being kept constant along the heavy ion track, is assumed in this paper [3].

Fig. 7. Id-Vd and Id-Vg curves of the PDK and TCAD models (Vd and Vg are the voltage of the drain and gate, respectively, and Id is the current of the drain).

Fig. 8(a) shows the TCAD model of the proposed RHEQ, where the x-z plane and the +y-axis are parallel and vertical to the surface of the cell, respectively. Meanwhile, the keywords θ and β are employed as the angle between the incident ion direction and the +y-axis and the angle between the projection direction of the incident ion in the x-z plane and the +x-axis with clockwise orientation, respectively [3]. The primary concerns in this paper are the SEU occurring on single node and SEMNUs caused by charge sharing among PMOSs in a single memory cell. Thus, to avert the effects of charge sharing between the off-NMOS and off-PMOS transistors, the Pc1, Pc2, Pb1, Pb2, NL1, and NR2 in proposed cell are built by TCAD models, and the others employed the SPICE models, as illustrated in Fig. 8(b). And the SET is acquired by heavy ions striking the PMOS TCAD model. Moreover, as the Q and X1 are the “same potential nodes”, the charge sharing efficiencies among the PMOS transistors can be evaluated by angle hit. The angle strike of 60° , which is broadly utilized to estimate the dependence that ion

Fig. 8. (a). TCAD model of the proposed RHEQ, (b). the top view of the proposed RHEQ schematic, and (c). the top view of the Quatro-10T schematic.

strike angle on SET [15, 16], thus, is also used in this work. By the above mixed-mode simulation, the influence of ion striking on the layout is studied under two situations which are demonstrated as follow.

Situation1: Assuming that the signals of proposed cell, $Q = '0'$, $QB = '1'$, $X0 = '1'$, $X1 = '0'$, $RWL = '0'$, and $WWL = '0'$, respectively. Thus, the Pc1, Pc2, Pb1, and Pb2 are in the off state, while the NL1 and NR2 are in the on state. Fig. 9 illustrates the simulation results that the heavy ion strikes on the drain of the corresponding off-PMOS with normal or angle hit. It is observed that the multiple-node upsets produced due to the charge sharing among PMOSs, and the proposed RHEQ cell can mitigate the influence of ion strike as an LET of $80 \text{ MeV-cm}^2/\text{mg}$ with the incident angle at 60° .

Situation 2: Assuming that the signals of proposed cell, $Q = '1'$, $QB = '0'$, $X0 = '0'$, $X1 = '1'$, $RWL = '0'$, and $WWL = '0'$, respectively. Thus, the Pc1, Pc2, Pb1 and Pb2 are in the on state, while the NL1 and NR2 are in the off state. Fig. 10 illustrates the simulation results that the heavy ion strikes on the drain of the corresponding off-NMOS with normal hit.

From Fig. 9 and Fig. 10, it can be deduced that the data of the proposed RHEQ will remain the original value when the single-event upset occurs on whichever single node of it, at $\text{LET} = 80 \text{ MeV-cm}^2/\text{mg}$. Due to the charge sharing of PMOSs has been considered in the mixed mode simulation, thus, the predictable conclusion is made that the SEMNUs caused by charge sharing among PMOSs can be mitigated in the proposed cell under ion striking with the value of LET equaling to $80 \text{ MeV-cm}^2/\text{mg}$.

Fig. 9. The simulation results of the node voltage versus time with $\text{LET} = 80 \text{ MeV-cm}^2/\text{mg}$.

Fig. 10. The simulation results of the node voltage versus time with $LET = 80 \text{ MeV-cm}^2/\text{mg}$.

As a supplement, the normal strikes with the LET values at $2 \text{ MeV-cm}^2/\text{mg}$, $10 \text{ MeV-cm}^2/\text{mg}$, $40 \text{ MeV-cm}^2/\text{mg}$, $70 \text{ MeV-cm}^2/\text{mg}$, and $100 \text{ MeV-cm}^2/\text{mg}$ have also been examined on the proposed SRAM cell. Due to the parasitic bipolar amplification effect of Pc1 mitigated by using stacked transistor, topology optimized, and layout-level design, thus, the charge collection of the Pc1 drain is reduced effectively. Therefore, the ion striking at the drain of the off-state transistor Pc2, Pb1 and Pb2 has little impact on the Q node, as shown in Fig. 11(b), (c) and (d), respectively. Meanwhile, as shown in Fig. 11, with the value of LET increasing, the pulse of SET is widened meaning that there is a much stronger disturbance in the memory cell. Nonetheless, the proposed RHEQ cell can still remain the original data at the value of the LET equaling to $100 \text{ MeV-cm}^2/\text{mg}$.

Moreover, we also carry out some work about SEU tolerance of the Quatro-10T. As the reference [4] mentioned, assuming $Q = '1'$, the redundant node X0 and the node Q could recover from $0 \rightarrow 1$ SET and $1 \rightarrow 0$ SET, respectively. Contrarily, $Q = '0'$, a sufficiently large $0 \rightarrow 1$ SET at node Q will flip the cell. Thus, the SEU tolerance efficiency of the Quatro-10T can be evaluated by striking the storage node Q (or QB). In this work, the PB, PC, NL1, and NR2 of the Quatro-10T are built by TCAD, as shown Fig. 8(c) and others use SPICE models. Assuming that the signals of the Quatro-10T, $Q = '0'$, $QB = '1'$, $X0 = '1'$, $X1 = '0'$, and $WL = '0'$, respectively. As shown in Table II and Fig. 12, the SEU threshold of it is between $1.3 \text{ MeV-cm}^2/\text{mg}$ and $1.4 \text{ MeV-cm}^2/\text{mg}$ with the normal strikes. As the reference [9] claimed that Quatro-10T has weak immune for SEMNUs because of charge sharing. As the simulation results demonstrated above, thus, compared with the Quatro-10T, the proposed memory cell has better SEU tolerance.

Fig. 11. The simulation results of the node voltage versus time with normal strikes at various LET values.

Table II. The effect of the storage data with normal striking the drains of the PC and Pc1 at different values of LET (Y and N are represent upset and not upset, respectively).

LET/MeV-cm ² /mg	0.5	0.9	1.3	1.4	2	10	20	40	80
Quatro-10T	N	N	N	Y	Y	Y	Y	Y	Y
Proposed RHEQ	N	N	N	N	N	N	N	N	N

Fig. 12. The simulation results of the node voltage versus time with normal strikes at $\text{LET} = 1.3 \text{ MeV-cm}^2/\text{mg}$ and $\text{LET} = 1.4 \text{ MeV-cm}^2/\text{mg}$.

4 Conclusion

This paper has proposed a radiation harden enhanced SRAM cell on the basis of the Quatro-10T, which is evaluated in 65 nm commercial technology. As compared with the Quatro-10T, this proposed cell shows greatly improved RM and WM, and has smaller write delay, less leakage current and lower dynamic power consumption. And the read delay of it is also acceptably. More importantly, the proposed SRAM cell can not only tolerate an SEU on any of its inner single nodes, but also have partial SEMNUs immune even at the LET value is equal to $80 \text{ MeV-cm}^2/\text{mg}$, which is better than that of the original Quatro-10T.

Acknowledgments

This work is supported by the National Natural Science Foundation of China (Grant No. 61674002, 61571012 and 61474001).