A 2–4 GHz fast-locking frequency multiplying delay-locked loop

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Abstract: A fast-locking fractional-ratio multiplying DLL (FMDLL) for de-skewed on-chip clock frequency multiplication is presented. A new phase detecting controller (PDC) and a dual-path charge pump (CP) have been adopted to achieve shorter locking time and eliminate lock-in fail problems. The proposed fast-locking FMDLL was implemented in a 65-nm CMOS process and occupies an active area of 0.015 mm\(^2\). It operates over a frequency range of 2.0–4.0 GHz with a programmable frequency multiplication factor of \(N/M\), where \(N = 4, 5, 8, 10\) and \(M = 1, 2, 3\). It achieves a peak-to-peak output clock jitter of 13.5 ps at 4 GHz while consuming 6.7 mW at 2 GHz from a 1.2 V supply. Compared with the conventional architecture, the locking time has been reduced about 80%.

Keywords: multiplying DLL, MDLL, frequency multiplier, clock generator, clock multiplier, fast locking, PLL, DLL

Classification: Integrated circuits

References


1 Introduction

The phase-locked loop (PLL) based clock generators and frequency multipliers have been widely used in integrated circuit design for microprocessors, digital system-on-chips (SoCs), and wireless communication transceivers [1, 2, 3, 4]. In recent years, multiplying delay-locked loops (MDLLs) [5, 6, 7, 8, 9, 10, 11] have been introduced as an alternative to conventional PLLs [1, 2, 3, 4]. An MDLL achieves better phase noise performance by periodically injecting a clean reference input clock to the delay line [5, 6, 7, 8]. MDLLs can generate integer-ratio [5, 6, 7, 8, 9, 10, 11] or fractional-ratio [12, 13] frequency multiplication. However, conventional integer-ratio [5, 6, 7, 8, 9, 10, 11] and fractional-ratio [12, 13] MDLL architectures have an unnecessarily long phase detecting period that causes longer locking time and even lock-in fail problems. The phase detecting and selecting structure of conventional MDLLs [5, 6, 7, 8, 9, 10, 11, 12] causes undesired charge pump charging current, resulting in increased locking time and even logical lock-in fails.

Nowadays, integrated clock generators and synthesizers require fast locking time for dynamic frequency switching and fast system power-mode transition. Therefore, locking time is one of the most important parameters in the design of clock generators and multipliers.

In this Letter, a fast-locking FMDLL with a new phase detecting controller (PDC) and a dual-path charge pump (CP) is presented to achieve shorter locking time and eliminate lock-in fail problems.

This Letter is organized as follows. Section 2 describes the phase detecting period and locking time problems of conventional MDLLs. Section 3 shows the architecture of the proposed fast-locking FMDLL and how to solve the critical
problems that existed in the previous structure. Section 4 shows the measurement results. Finally, Section 5 gives conclusion.

2 Phase detecting period and locking time issue

Fig. 1(a) shows the architecture of conventional MDLL [5], which consists of a 2:1 multiplexer (MUX), a phase detector (PD), a charge pump (CP), a voltage controlled delay line (VCDL), select logic, and a divide by N divider. Fig. 1(b) depicts the locking process and phase detecting period with a frequency multiplication factor of $N = 4$. The phase detecting period ($t_{PDP}$) is defined by the Sel signal which is generated by the select logic and activated high from the $N$th falling edge of CLKOUT to the rising edge of the next CLKIN, where CLKIN is the input and CLKOUT is the output clock, respectively. The Sel signal is used to control the 2:1 MUX and the PD. Since the MDLL starts with its minimum delay, the problem is that the pulse width of $t_{PDP}$ can become longer than half of the CLKIN period. In this situation, the PD generates two CP control signals (UP and DN) simultaneously, where UP is used to charge up and DN is used to discharge the CP in the combined phase detector and charge pump circuit in [5]. In Fig. 1(b), the VCDL delay should be increased by lowering the $V_{Cut}$ voltage for proper locking. However, the undesired UP pulses increase the $V_{Cut}$ voltage (Actual signal), which increases the locking time seriously and even causes lock-in fails. Therefore, this kind of phase detecting and CP control scheme is not proper to use in applications where fast locking is required for frequency multiplication.

3 Proposed architecture and circuit design

Fig. 2(a) shows a block diagram of the proposed fast locking FMDLL with deskewed fractional-ratio frequency multiplication capability. It consists of a 3-to-1 MUX, a VCDL, two programmable frequency dividers ($/M$ and $/N$), a MUX controller, a dual-path charge pump, and a new phase detecting controller (PDC). The proposed FFMDLL provides multiplied fractional-ratio output clock $f_{clk_{out}} = f_{clk_{in}} \times (N/M)$, where $N$ and $M$ are integer and programmable and $f_{clk_{out}}$ and $f_{clk_{in}}$ are the frequencies of CLKOUT and CLKIN, respectively. The PDC includes a
PD and a new PD/CP control logic. The PDC is used to define a new $t_{\text{PDP}}$ window and boost the CP discharge current for fast locking. Fig. 2(b) shows the proposed PD/CP control logic and dual-path CP. The PD/CP control logic is implemented by using dynamic CMOS gates and generates two control signals, Sel$_{\text{PD}}$ and DN2. When the Sel$_{\text{PD}}$ signal is enabled high, the PD compares the two input clock signals, CLK$_{\text{IN}}$ and CLK$_{\text{OUT}}$, and generates UP or DN1 signals depending on the phase difference of the two input clocks.

The MUX controller is similar to the one used in [12]. Similar to [12] and [13], the proposed FMDLL has three operation modes for N/M frequency multiplication: ring oscillator (RO), reference injection (RI), and supply injection (SI).

Fig. 3 shows the detailed locking process of the proposed FMDLL with $N/M = 8/3$. In conventional MDLL [5], the $t_{\text{PDP}}$ window is defined by the Sel[0] signal. Since the Sel[0] is activated high from the $N$th falling edge of CLK$_{\text{OUT}}$ to the $(M+1)^{\text{th}}$ rising edge of CLK$_{\text{IN}}$, the unnecessarily large $t_{\text{PDP}}$ window generates undesired UP pulses that increases the locking time.

The proposed PD/CP control logic, shown in Fig. 2(b), generates the Sel$_{\text{PD}}$ signal to activate the PD. The Sel$_{\text{PD}}$ signal becomes high when all the CLK$_{\text{IN}}$, CLK$_{\text{OUT}}$, DIV$_{\text{N}}$, and DIV$_{\text{M}}$ signals are low. During the $t_{\text{PDP}}$ window, the phase of the CLK$_{\text{IN}}$ and CLK$_{\text{OUT}}$ are compared by the PD and the PD generates the UP or DN1 signals to control the charging/discharging current paths of the CP.

In Fig. 3, the DN1 is enabled high since the CLK$_{\text{OUT}}$ leads CLK$_{\text{IN}}$ during the $t_{\text{PDP}}$ window. Compared with the previous $t_{\text{PDP}}$ window defined by the Sel[0], the
new t_PDP window has become much narrow. In the previous scheme, the undesired UP pulse can be activated high if the third rising edge of CLK_{IN} leads the first rising edge of CLK_{OUT} during the high pulse on Sel[0]. However, the PD is enabled only when the Sel_{PD} signal is high (new t_PDP window) in the proposed scheme, the undesired UP pulses can be eliminated. Also, the PD/CP control logic generates the DN2 signal to enable the fast discharging path of the CP. The DN2 signal is activated high when the Sel_{PD} signal is low and the Sel[0] signal becomes high. The DN2 signal is deactivated when the Sel_{PD} signal becomes high. The high pulse on DN2 is used to reduce the locking time at the beginning of the operation.

Fig. 3. Locking process of the proposed FMDLL with new t_PDP window

Fig. 4(a) shows the operation of the dual-path CP using the dual-slope V_{ctrl} signal. If the t_{DL} is larger than t_{cyc}/2 at the beginning of the operation, both the first and second discharging paths of the CP are turned on. Here the t_{DL} is defined as the required VCDL delay for proper phase locking (see Fig. 6). During this period, the V_{ctrl} voltage drops quickly due to the two discharging current summation of I_{DN1} + I_{DN2}, resulting in faster VCDL delay increase. Then when the t_{DL} becomes smaller than t_{cyc}/2, only the first discharging path (I_{DN1}) of the CP is turned on and

![Diagram of CLKIN, CLKOUT, DivM, DivN, Sel[0], Sel_{PD}, DN1, UP, DN2, V_{ctrl}](image)

![Diagram of V_{ctrl} signal and locking time comparison](image)
the Vctrl voltage drops slowly. When the Vctrl voltage reaches the locking point, only the first charging/discharging path \((I_{UP} + I_{DN1})\) can be turned on depending on the phase error and therefore the Vctrl voltage remains constant to keep phase locking. As a result, the use of the dual-path CP and the new PDC effectively reduces the locking time.

Fig. 4(b) shows the comparison of locking time at 2 GHz. Compared with the conventional scheme using a simple PD and CP, the proposed scheme using the dual-path CP and a PDC achieves a locking time reduction of about 80%.

4 Experiment results

The proposed FFMDLL is fabricated in a 65 nm CMOS process. Fig. 5 shows the chip microphotograph and layout of the proposed FFMDLL. It occupies an active area of only 0.015 mm². The clock waveforms and peak-to-peak (pk-pk) jitter characteristics are measured using the sampling oscilloscope Tektronix DSA71604. The network analyzer (Agilent E4445A) is used for measuring the phase noise, reference spur, and the integrated RMS jitter.

Fig. 6 shows the simulated locking process that illustrates the operation of PDC more in detail when \(N/M = 10/3\). As already illustrated in Fig. 3, the FMDLL operates with repeated mode transitions from RO \(\rightarrow\) SI \(\rightarrow\) RI. After locking, only RI and RO modes are repeated just like the conventional MDLLs.

Fig. 7(a) shows the measured input and output clock waveforms at the initial and after locking points at 4 GHz with \(N/M = 10/2\). It is clearly shown that
fractional-ratio frequency multiplication is realized and the phases of CLK\textsubscript{IN} and CLK\textsubscript{OUT} are aligned well with no skew after locking. Fig. 7(b) shows the measured pk-to-pk output clock jitter of 13.5 ps at 4 GHz with $N/M = 10/2$ (left) and 3 GHz with $N/M = 8/3$ (right).

![Fig. 7. (a) Measured input and output clock signals at initial and after locking with $N/M = 10/2$ (b) Measured output clock pk-to-pk jitter at 4 GHz with $N/M = 10/2$ (left) and 3 GHz with $N/M = 8/3$ (right).](image)

Fig. 8 shows the measured noise performance when $f_{clk_{out}} = 4$ GHz and $N/M = 10/2$ (a) Measured reference spur, (b) Measured phase noise.

![Fig. 8. (a) Measured noise performance when $f_{clk_{out}} = 4$ GHz and $N/M = 10/2$ (a) Measured reference spur, (b) Measured phase noise.](image)

Fig. 8 shows the measured noise performance when $f_{clk_{out}} = 4$ GHz and $N/M = 10/2$. As shown in Fig. 8(a), the measured reference spur is $-33.82$ dBc/Hz. In Fig. 8(b), the measured phase noise is $-120.8$ dBc/Hz at 1 MHz offset. The proposed FMDLL consumes 6.7 mW at 2 GHz and 12.6 mW at 4 GHz, respectively.
A performance comparison of the proposed fast-locking FMDLL and state-of-the-art analog MDLL-based clock frequency multipliers is given in Table I. The comparison shows that the proposed FMDLL achieves good jitter and noise performance while maintaining faster locking time and de-skewed fractional-ratio frequency multiplication capability.

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<th>Table I. Performance summary and comparison with state-of-the-art MDLL-based clock frequency multipliers</th>
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5 Conclusion

A 2–4 GHz fast-locking fractional-ratio frequency multiplying DLL (FMDLL) has been implemented in a 65 nm CMOS process. The proposed fast-locking FMDLL adopts a new phase detecting controller and a dual-path charge pump to achieve shorter locking time and eliminate lock-in fail problems. The proposed FMDLL operates over a frequency range of 2.0–4.0 GHz with a programmable frequency multiplication ratio of N/M, where N = 4, 5, 8, 10 and M = 1, 2, 3. Compared with the conventional MDLL-based architecture, the proposed FMDLL achieves an locking time reduction of 80%. With an active area of only 0.015 mm², it also achieves a measured pk-pk output clock jitter of 13.5 ps at 4 GHz.

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