Enhanced 3 x VDD-tolerant ESD clamp circuit with stacked configuration

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Abstract: An enhanced 3 x VDD-tolerant ESD clamp circuit with stacked configuration was presented. Four transistors were added in this design to transfer bias voltages or ESD voltages. This circuit was simulated in 0.18 µm silicon-on-insulator (SOI) CMOS process and 28 nm HKMG CMOS technology. Spectre-simulation results showed that the ESD discharge current is increased by 2 times and the discharge current is decreased to nA magnitudes compared to the conventional circuit.

Keywords: electrostatic discharge (ESD), power clamp, mixed-voltage I/O, high discharge current, SOI CMOS process, 28 nm high-k CMOS process

Classification: Electron devices, circuits and modules

References


1 Introduction

With the development of CMOS process, the thickness of gate-oxide has been scaled down and the power supply has been decreased to improve circuit performance [1, 2]. In the ICs whole system integration, I/O buffers with low voltage devices drive or receive high-voltage signals when they communicate with other ICs. And the overstress voltage is an important parameter in I/O buffers with thinner gate oxide [3, 4]. To solve gate-oxide reliability issue without using additional masks and special devices, the three-stage stacked NMOS configuration of a RC-triggered power clamp circuit is widely used in the mixed-voltage I/O buffers. However, the small electrostatic discharge (ESD) robustness and large leakage current lower its performance [5, 6, 7]. In this report, an enhanced ESD protection design for the 3 × VDD-tolerant mixed-voltage I/O buffer is proposed. It was also simulated in 0.18 μm silicon-on-insulator (SOI) CMOS technology and the Semiconductor Manufacturing International Corporation (SMIC) 28 nm HKMG (high-k metal-gate) CMOS technology, respectively.

2 Conventional three-stage stacked NMOS configuration

A conventional three-stage stacked NMOS configuration [8, 9, 10, 11] is shown in Fig. 1. Under normal circuit operation, \( V_A \) (voltage on node A) = \( V_{B0} = 2VDD \), \( V_B \) (voltage on node B) = \( V_{B1} = VDD \), \( V_C \) (voltage on node C) = 0. In this condition, the big NMOS transistors M0, M1 and M2 are turned off. Under positive ESD stress, the RC detection circuit can’t follow the change of the voltage on ESD bus. Thus, node d, e and f are kept in low voltage state and node A, B and C are charged to high voltages.

In this case, the big NMOS transistors M0, M1 and M2 are turned on to discharge ESD current. The on-resistance \( r_{on} \) of big NMOS transistors can be expressed as

\[
r_{on} = \frac{1}{\mu C_{OX} \left( \frac{W}{L} \right) (V_{GS} - V_{TH})}.
\]

where \( (V_{GS} - V_{TH}) \) is the overdrive voltage, \( W \) and \( L \) represent the big NMOS transistors’ width and length respectively. The low ESD discharge current is mainly
caused by the large on-resistance of big NMOS transistors in conventional stacked configuration. Therefore, it’s favorable to have a high enough overdrive voltage of the big NMOS transistors to limit the $r_{on}$. A modified $3 \times VDD$-tolerant ESD clamp circuit is shown in section 3, which can increase overdrive voltages and reduce leakage current.

### 3 Proposed $3 \times VDD$-tolerant ESD clamp circuit

![Fig. 1. The conventional three-stage stacked ESD clamp circuit.](image)

The proposed enhanced $3 \times VDD$-tolerant ESD clamp circuit is shown in Fig. 2. The RC time constant is around $\sim 1 \text{us}$ to distinguish ESD stress events from the normal circuit operating condition. Four NMOS transistors MN0, MN1, MP0 and MP1 were added to increase the overdrive voltages of the big NMOS transistors M0, M1 and M2. Under normal condition, MP0 and MP1 are turned on to transfer bias voltages. Therefore, big NMOS transistors are kept in off state. Under positive ESD stress, MN0 and MN1 are turned on to transfer the high voltage on ESD bus. Then the $V_{GS}$ of big NMOS transistors can be kept in high voltages to discharge ESD current. To reduce leakage current, the diode-connected PMOS transistors are replaced by NMOS transistors whose gate and source are connected together.

1) Under normal circuit operation, the NMOS transistors (MN2~MN7) are used as the voltage dividers to bias the three ESD detection circuits. Then $V_{B0} = 2VDD$, $V_{B1} = VDD$ and the voltages of nodes f, g and h are 3VDD, 2VDD and VDD. Thus, MN8 and MN9 are kept in on state and pull the voltages of nodes i, j down to VDD and 0 V respectively. MP0 and MP1 are turned on to keep the voltage level of node d, e biased at voltage $V_{B0}$ and $V_{B1}$. The voltage level of node A, B and C are 2VDD, VDD and 0 V. Then all big NMOS transistors in the enhanced topology are kept in off state due to $V_{GS} = 0 \text{V}$. Since voltages between each two adjacent nodes of devices do not exceed VDD, the ESD circuit is free from the gate-oxide reliability issue under normal condition.
2) When a positive ESD stress is applied to the 3 × VDD ESD bus, the RC detection circuit can’t follow the voltage’s change on ESD bus. Then node f is kept in low voltage and node A is kept in high voltage. Owing to the high gate voltage, MN0 is turned on to transfer the high voltage to node d. Subsequently, MP9 and MN1 are turned on. Due to the low current in MP8 and MP9, their source-to-drain voltages $V_{SDP}$ are nearly zero. In addition, the drain-to-source voltages $V_{DSN}$ of MN0 and MN1 are around $V_{THn}$. The gate-to-source voltage of M2 is promoted from $3VDD-V_{SDP}$ in the conventional circuit to $3VDD-2V_{DSN}-V_{SDP} \approx 3VDD-2V_{THn}-V_{SDP}$. The gate voltages of M1 and M0 are $3VDD-V_{DSN}-V_{SDP} \approx 3VDD-V_{THn}$ and $3VDD-V_{SDP} \approx 3VDD$, which are only $2VDD-V_{SDP}$ and $3VDD-V_{SDP}$ in conventional circuit.

Refer to equation (1), in the proposed circuit the on-resistances ($r_{on}$) of big NMOS transistors (M1, M2) are reduced due to larger gate voltages, though the dimensions remain the same. The reduced on-resistances ($r_{on}$) make the voltage level on node k decrease. Then the $V_{GS}$ of M0 working in saturation region can be increased. Therefore, the discharge current can be expressed as

$$i = \frac{1}{2} \mu_n C_{OX} \left( \frac{W}{L} \right) (V_{GS} - V_{TH})^2. \quad (2)$$

where $V_{GS}$ of M0 is effectively increased from $VDD-V_{SDP}$ (in conventional circuit) to $3VDD-V_{DSM1}-V_{DSM2}$ (in the proposed circuit).

4 Simulation results

4.1 Proposed stacked ESD clamp circuit in 28 nm HKMG 1.8 V CMOS process

In advanced 28 nm HKMG CMOS process, devices with thinner gate oxides could be easily damaged by ESD stress. To verify the enhanced robustness in this ESD clamp circuit, a 0–6 V ESD-like voltage pulse (the rise time is 10 ns) is applied to the internal ESD bus. The RC time constant is 0.96 us. The simulated results are...
shown in Fig. 3.

Under positive ESD condition, the discharge current is increased from 1.75 A in the conventional circuit to 3.48 A in the proposed circuit as shown in Fig. 3(a).

![Simulated results of proposed clamp circuit under positive ESD condition in 28 nm high-k CMOS technology.](image)

**Fig. 3.** (a) Simulated results of proposed clamp circuit under positive ESD condition in 28 nm high-k CMOS technology. (b) Simulated results of proposed clamp circuit under normal operation in 28 nm high-k CMOS technology.

Currents of MP0/1, and MN0/1 are 18 nA, 110 µA. Transistors MP0/1 are kept in off state and transistors MN0/1 are kept in on state. The voltage levels of node A, B and C are 6 V (3VDD), 5.48 V (≈3VDD-V_{THn}) and 4.97 V (≈3VDD-2V_{THn}-V_{SDp}). The start-up time is 5.4 ns as shown in Fig. 3(a) inset if the turn-on current was set as 20 mA. This circuit can turn on timely. In addition, the delay time for the current to reach 1.75 A is promoted from 10.64 ns in the conventional circuit to 8.75 ns in the enhanced one, indicating a faster turn-on speed.

Under normal condition, Fig. 3(b) shows that the voltage values of internal ESD bus, node A, B, C, k and m are 5.4 V, 3.6 V, 1.8 V, 0 V, 3.6 V and 1.8 V respectively. The big NMOS transistors are turned off. The leakage current (I₁) caused by dividers is only 2 pA and the total leakage current is reduced from 64 µA (I_{con}) in conventional circuit to 22 nA (I_{pre}) in proposed circuit. This circuit has been simulated under different corners: ff, tt, ss. The max and minimum discharge currents are 3.61 A and 3.34 A respectively. The dimensions of R, C, transistors MP0, MP1, MN0 and MN1 are shown in Table I. This proposal ESD circuit is
aimed to meet HBM-2kV (Human Body Mode) and MM-200V (Machine Mode).

4.2 Proposed stacked ESD clamp circuit in 0.18 µm SOI 2.5 V CMOS

Table I. Dimensions of devices of the conventional and proposed circuits

<table>
<thead>
<tr>
<th>Devices</th>
<th>Dimensions of conventional circuit</th>
<th>Dimensions of proposed circuit</th>
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<tbody>
<tr>
<td></td>
<td>W/L</td>
<td>M</td>
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<tr>
<td>MP0</td>
<td>×</td>
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<td>MP1</td>
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<tr>
<td>MN0</td>
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<tr>
<td>MN1</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>Big NMOS</td>
<td>104.8 µm/320 nm</td>
<td>30</td>
</tr>
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</table>

R = 520 kΩ, C = 1.86 pF

process

In 0.18 µm SOI 2.5 V CMOS process, the thinner gate oxide and shallower diffusion junction depth seriously degrade the ESD robustness of integrated circuits, and raise the difficulty for ESD protection design. The dimensions of devices in conventional and proposed circuits are shown in Table II.

A 0–8 V ESD-like voltage pulse (the rise time is 10 ns) is applied to the internal ESD bus to simulate the ESD transient voltage. The simulated results show that the discharge current is increased from 2.14 A in the conventional circuit to 4.82 A in the proposed circuit under positive ESD condition. The voltage levels of internal ESD bus, node A, B and C are 8 V, 8 V, 7.26 V and 6.5 V. The currents of transistors MP0/1, and MN0/1 are 83 nA, 666 µA. This circuit has been simulated under different corners: ff, tt, ss. The max and minimum discharge currents are 5.09 A and 4.49 A respectively. The start-up delay time of this enhanced circuit is just 3.9 ns as shown in Fig. 4(a) inset. This circuit can turn on timely. The delay time for the current to reach 2.14 A is promoted from 10.21 ns in the conventional circuit to 8.76 ns in the enhanced one, indicating a faster turn-on speed.

Under normal circuit operation, the voltage levels of internal ESD bus, node A, B and C are shown in Fig. 4(b). The big NMOS transistors are kept in off state. And the leakage current caused by the dividers (NMOS transistors) is only 81 pA far less than 106.1 µA in conventional circuit. And the total leakage current of this proposed circuit is just 37 nA. This enhanced circuit’s ESD level is speculated to be
kept between HBM 4 KV to 8 KV.

5 Conclusion

In this paper, an enhanced stacked ESD clamp circuit is proposed to keep low leakage currents under normal circuit operation. This modified circuit was simulated in 28 nm HKMG CMOS technology and 0.18 µm SOI CMOS process to verify the promoted ESD robustness. In both processes, the discharge current in the proposed circuit is 2 times higher than the conventional circuit.

Acknowledgments

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