A novel high performance 3×VDD-tolerant ESD detection circuit in advanced CMOS process

Xiaoyun Li, Houpeng Chen^{a)}, Yu Lei^{b)}, Qian Wang, Xi Li, Jie Miao, and Zhitang Song

State Key Laboratory of Functional Materials for Informatics; Shanghai Institute of Micro-system and Information Technology, Chinese Academy of Sciences; University of Chinese Academy of Sciences, Shanghai 200050, China

a) chp6468@mail.sim.ac.cn

b) leiyuthuniverse@gmail.com

Abstract: A novel high performance 3×VDD-tolerant electrostatic discharging (ESD) detection circuit using only 1×VDD devices was presented in a 28 nm 1.8 V high-k metal-gate (HKMG) CMOS technology. A sub-path and an enhanced path were adopted in this novel design to increase its trigger current. Two small-sized PMOS transistors were employed to protect this circuit out of gate-oxide reliability issues under normal operating conditions. And there is only one capacitor in our novel circuit to maintain a small layout area. Under the ESD stress events, spectre-simulation results show that the trigger current of our proposed circuit can reach 36.4 mA. And its leakage current is only 2.8 nA at 27°C, 243 nA at 120°C under normal operating conditions.

Keywords: electrostatic discharge (ESD), mixed-voltage I/O, high trigger current, detection circuit, 28 nm HKMG CMOS process

Classification: Electron devices, circuits and modules

References

- [1] M. D. Ker and C. T. Wang: "Design of high-voltage-tolerant ESD protection circuit in low-voltage CMOS processes," *IEEE Trans. Device Mater. Rel.* **9** (2009) 49 (DOI: [10.1109/TDMR.2008.2008639](https://doi.org/10.1109/TDMR.2008.2008639)).
- [2] K. Yu, *et al.*: "Enhanced ESD power clamp for antenna switch controller with SOI CMOS technology," *Electron. Lett.* **51** (2015) 871 (DOI: [10.1049/el.2014.4160](https://doi.org/10.1049/el.2014.4160)).
- [3] M. D. Ker and C. Y. Lin: "High-voltage-tolerant ESD clamp circuit with low standby leakage in nanoscale CMOS process," *IEEE Trans. Electron Devices* **57** (2010) 1636 (DOI: [10.1109/TED.2010.2049072](https://doi.org/10.1109/TED.2010.2049072)).
- [4] C.-T. Yeh and M.-D. Ker: "New design on 2×VDD-tolerant power-rail ESD clamp circuit with low standby leakage in 65 nm CMOS process," 2012 International Symposium on VLSI Design, Automation, and Test (VLSI-DAT) (2012) 1 (DOI: [10.1109/VLSI-DAT.2012.6212606](https://doi.org/10.1109/VLSI-DAT.2012.6212606)).
- [5] S. Athanasiou, *et al.*: "Reconfigurable ultra-thin film GDNMOS device for ESD protection in 28 nm FD-SOI technology," *Solid-State Electron.* **128**

- (2017) 172 (DOI: [10.1016/j.sse.2016.10.026](https://doi.org/10.1016/j.sse.2016.10.026)).
- [6] C.-Y. Lin, *et al.*: “Improving ESD robustness of pMOS device with embedded SCR in 28-nm high-k/metal gate CMOS process,” IEEE Trans. Electron Devices **62** (2015) 1349 (DOI: [10.1109/TED.2015.2396946](https://doi.org/10.1109/TED.2015.2396946)).
 - [7] C. Duvvury, *et al.*: “Achieving uniform nMOS device power distribution for sub-micron ESD reliability,” Tech. Dig. IEDM (1992) 92 (DOI: [10.1109/IEDM.1992.307325](https://doi.org/10.1109/IEDM.1992.307325)).
 - [8] M.-D. Ker and C.-T. Wang: “ESD protection design by using only $1\times V_{DD}$ low-voltage devices for mixed-voltage I/O buffers with $3\times V_{DD}$ input tolerance,” Solid-State Circuits Conference, ASSCC (2006) 287 (DOI: [10.1109/ASSCC.2006.357907](https://doi.org/10.1109/ASSCC.2006.357907)).
 - [9] H. Liu, *et al.*: “Two ESD detection circuits for $3\times V_{DD}$ -tolerant I/O buffer in low-voltage CMOS processes with low leakage currents,” IEEE Trans. Device Mater. Rel. **13** (2013) 319 (DOI: [10.1109/TDMR.2012.2218606](https://doi.org/10.1109/TDMR.2012.2218606)).
 - [10] X. Li, *et al.*: “Enhanced $3\times V_{DD}$ -tolerant ESD clamp circuit with stacked configuration,” IEICE Electron. Express **14** (2017) 20160901 (DOI: [10.1587/elex.14.20160901](https://doi.org/10.1587/elex.14.20160901)).
 - [11] M.-D. Ker and K.-C. Hsu: “Overview of on-chip electrostatic discharge protection design with SCR-based devices in CMOS integrated circuits,” IEEE Trans. Device Mater. Rel. **5** (2005) 235 (DOI: [10.1109/TDMR.2005.846824](https://doi.org/10.1109/TDMR.2005.846824)).
 - [12] M. Elghazali, *et al.*: “A low-leakage, robust ESD clamp with thyristor delay element in 65 nm CMOS technology,” IEEE Computer Society Annual Symposium on VLSI (ISVLSI) (2016) 421 (DOI: [10.1109/ISVLSI.2016.57](https://doi.org/10.1109/ISVLSI.2016.57)).

1 Introduction

For whole system integration, I/O buffers with low voltage devices will drive or receive high-voltage signals when they communicate with other ICs [1, 2]. The $3\times V_{DD}$ -tolerant ESD power clamp circuit is composed of an ESD detection circuit and an ESD device [3, 4]. The detection circuit can distinguish ESD stress events from the normal circuit operating conditions and trigger the ESD device effectively.

However, with the advancing of CMOS technology, the thickness of gate-oxide has been scaled down and the power supply has been decreased to improve circuit performance which limited the ESD design window [5, 6]. And some advanced processes seriously increase the difficulty of ESD protection design and degrade the ESD robustness, such as Lightly-Doped Drain (LDD) process and silicide process [7, 8]. Therefore, an efficient ESD detection circuit is required to improve the ESD robustness.

2 Conventional $3\times V_{DD}$ -tolerant ESD detection circuits

In the previous researches, many different kinds of $3\times V_{DD}$ -tolerant ESD detection circuits have been proposed, such as a $3\times V_{DD}$ -tolerant ESD detection circuit with deep N-well structure to avoid the gate-oxide overstress between the gate and the bulk (Circuit A) in Ref. [1], a $3\times V_{DD}$ -tolerant ESD detection circuit with an additional control path (Circuit B) in Ref. [1], a $3\times V_{DD}$ -tolerant ESD detection circuit using three stacked capacitors and a resistor as its RC network (Circuit A) [9] and a $3\times V_{DD}$ -tolerant ESD detection circuit with a novel bias circuit applying three capacitors and two NMOS transistors to keep its leakage current low

(Circuit B) [9], etc. These circuits will be compared with our proposed circuit in Section 5.

3 The proposed $3\times VDD$ -tolerant ESD detection circuit

The structure of our proposed ESD detection circuit and its ESD device is shown in Fig. 1. R_0 and C_0 form the RC network which can distinguish ESD stress events from the normal operating conditions [10]. The RC time constant is around $1\ \mu s$. The three identical transistors (MN4~MN6) form the bias circuit to bias nodes “d”, “f” at $2VDD$ and VDD , respectively, under normal operating conditions. The gates of MN4~MN6 are all connected with their own sources to keep themselves in off state. So the leakage current of this bias circuit can be very low. The stacked transistors MP5~MP7 and R_1 compose a sub-path which is controlled by the RC network. This sub-path can control the voltage of node “g”. Transistors MP3 and MP4 turn on to make $V_B = V_d = 2VDD$, $V_C = V_f = VDD$ under normal operating conditions. Therefore, transistors MN1~MN3 and MP0~MP2 can be protected out of gate-oxide reliability issues. MN1~MN3 form the enhanced path to decrease the voltages of nodes “A”, “B” “C” and MP0~MP2 form the trigger path to generate the trigger current.

The ESD device in this novel detection circuit is a SCR device [11] with m diodes in series. The value of m depends on the manufacturing process. The mechanism of our proposed detection circuit is described in detail in below.

Fig. 1. The novel $3\times VDD$ -tolerant ESD detection circuit with the ESD device.

3.1 Mechanism of our novel detection circuit under the ESD events

To detailed describe the operation of our proposed circuit under the ESD events, it can be split into four phases.

- 1) In phase1, $V_{BUS} - V_A \leq |V_{THP}|$, all of the transistors except MP3 and MP4 are kept in off state. MP3 and MP4 may turn on or work in the sub-threshold region due to the bias voltage of nodes “d” and “f”. Node “A” is charged

quickly by the high voltage on ESD_BUS line. This operating phase is shown in Fig. 2(a). The symbols “×” and “√” represent transistors’ on and off states, respectively.

- 2) In phase 2, when $V_{BUS} - V_A \geq |V_{THP}|$, $V_{id} < |V_{THP}|$ and $V_{ef} < |V_{THP}|$, MP5 and MP0 turn on. MP6 and MP7 are kept in off state. There is a small current in the sub-path. Nodes “i”, “e” and “g” are charged slowly. V_g is still less than V_{THN} . This operating phase is shown in Fig. 2(b).
- 3) In phase 3, with the charging of node “g”, when $V_g \geq V_{THN}$, MN3 turns on. In this phase, MN2 and MN1 have not yet turned on as shown in Fig. 2(c).

Fig. 2. (a) Phase 1; (b) Phase 2; (c) Phase 3; (d) Phase 4 of our proposed 3×VDD-tolerant ESD detection circuit under the ESD event.

- 4) In phase 4, with the turning on of MN3, MN2 and MN1 turn on successively. Then the enhanced path turns on to discharge the voltages of nodes “A”, “B” and “C” down to VSS (0 V). The equivalent resistances (r_{p0} , r_{p1} , r_{p2}) of trigger transistors MP0~MP2 can be expressed as

$$r = \frac{1}{\mu_p C_{OX} \left(\frac{W}{L} \right) (V_{SG} - |V_{THP}|)} \quad (1)$$

where $(V_{SG} - |V_{THP}|)$ is the overdrive voltage, W and L represent the trigger transistors' width and length, respectively.

The lower gate voltages (V_A , V_B , V_C) can increase the source-to-gate voltages of MP0~MP2. And their equivalent resistances (r_{p0} , r_{p1} , r_{p2}) become smaller with the increasing of their source-to-gate voltages. Therefore, the trigger transistors MP0~MP2 can generate a large trigger current I_{tri} . Moreover, the low gate voltage (V_C) can make MN0 completely turn off to eliminate the current consumed by MN0. Then the large trigger current can totally flow to the P-well/P-sub resistance (R_d) of the ESD device as shown in Fig. 2(d).

As a result, the trigger current of this proposed circuit can be enhanced and the enhanced trigger current can trigger the ESD device earlier. In this phase, the sub-path turns on to charge nodes “i”, “e”, “g” quickly. $V_{de} < |V_{THP}|$ and $V_{fg} < |V_{THP}|$, MP3 and MP4 turn off.

3.2 Mechanism of our novel detection circuit under normal operating conditions

Under normal operating conditions, transistors MN4~MN6 bias V_d , V_f at $2V_{DD}$ and V_{DD} . The RC network follows the voltage change of V_{BUS} . $V_A = V_{BUS} = 3V_{DD}$, MP5 turns off. The sub-path is kept in off state. So $V_{id} < |V_{THP}|$, $V_{ef} < |V_{THP}|$, MP6 and MP7 are kept in off state. The three off-state transistors MP5~MP7 are equivalent to three infinite resistors (R_e) in series. $R_e \gg R_1$. Therefore, V_{BUS} is trisected by MP5~MP7. Then $V_g \approx V_{SS}$ and $V_e \approx V_{DD}$, the enhanced path is kept in off state. $V_{de} = V_{fg} = V_{DD}$, transistors MP3 and MP4 turn on to make $V_B = V_d = 2V_{DD}$, $V_C = V_f = V_{DD}$. Therefore, transistors MN1~MN3 and MP0~MP2 can be protected out of gate-oxide reliability issues. MP0 turns off because its $V_{SG} = V_{BUS} - V_A = 0$ V. Then the trigger path is kept in off state. MN0 turns on due to its $V_{GS} = V_{DD}$. Therefore, $V_h = V_{SS}$ (0 V) and the ESD device is kept in off state.

4 Simulation results

This novel ESD detection circuit is verified in a 28 nm HKMG 1.8 V CMOS technology. In advanced 28 nm HKMG CMOS technology, devices with thinner gate oxides could be easily damaged by ESD stress. According to the PDK files which is provided by the foundry, the gate-oxide breakdown voltage of the 1.8 V MOSFET devices is 9.36 V and $V_{THN} = 0.58$ V, $|V_{THP}| = 0.41$ V.

To verify the performance of the proposed ESD detection circuit, a 0–6 V ESD-like voltage pulse (the rise time is 10 ns) is applied to the internal ESD bus. A 100 Ω resistance is added between node “h” and VSS to simulate the P-well/P-sub resistance of SCR device [9].

4.1 Spectre-simulation results

Under the ESD events, the voltage waveforms of our proposed ESD detection circuit are shown in Fig. 3. The operation is split into four phases as described in section 3.1.

- 1) In phase 1, $V_{BUS} - V_A \leq |V_{THP}|$ ($= 0.41$ V), 10 ns $\leq t \leq 13.6$ ns. In this phase, $V_{SG,MP5} = V_{SG,MP0} < |V_{THP}|$, $V_{id} < |V_{THP}|$, $V_g < V_{THN}$, the sub-path, the trigger path and the enhanced path are in off state. When $t = 13.6$ ns, $V_{BUS} - V_A = 0.41$ V. $V_{id} = 0.10$ V, $V_{ef} = 0.21$ V and $V_g = 0.50$ V. At this point, MP3 turns on and MP4 works in sub-threshold region due to $V_{de} = 0.55$ V, $V_{fg} = 0.31$ V. Node “A” is charged to 1.76 V.
- 2) In phase 2, $V_{BUS} - V_A \geq |V_{THP}|$ and $V_g \leq V_{THN}$, 13.6 ns $\leq t \leq 13.9$ ns. In this phase, $V_{id} < |V_{THP}|$ (0.41 V), $V_{ef} < |V_{THP}|$ (0.41 V), MP6 and MP7 are kept in off state. There is a small current in the sub-path due to the turning on of MP5. When $t = 13.9$ ns, the voltage of nodes “i”, “e” and “g” are charged to 2.06 V, 1.28 V, 0.58 V, respectively.
- 3) In phase 3, $V_g \geq V_{THN}$, $V_{fc} \leq V_{THN}$, and $V_{dB} \leq V_{THN}$, 13.9 ns $\leq t \leq 14.2$ ns. MN3 turns on, MN2 and MN1 have not yet turned on. When $t = 14.2$ ns, MN2 is in the critical open state. $V_A = 1.98$ V, $V_B = 1.38$ V, $V_C = 0.4$ V. At this point, MP6 and MP7 turn on due to $V_{id} = 0.46$ V $> |V_{THP}|$, $V_{ef} = 0.43$ V $> |V_{THP}|$. MP1 and MP2 turn on due to $V_{SG,MP1} = V_{SG,MP2} = 0.52$ V $> |V_{THP}|$. MP3 turns on and MP4 works in sub-threshold region due to $V_{de} = 0.55$ V, $V_{fg} = 0.32$ V.
- 4) In phase 4, $t > 14.2$ ns. With the turning on of MN3, MN2 and MN1 turn on successively. Then the enhanced path turns on to discharge the voltages on node “A”, “B” and “C” down to 3.10 mV, 1.72 mV and 0.75 mV. The low gate voltages (V_A , V_B , V_C) make MN0 turn off to decrease the current consumed by MN0 (3.27 μ A) and make the trigger transistors MP0~MP2 completely turn on to generate a large trigger current (36.4 mA). MP3 and MP4 turn off due to $V_{de} < 0$ V, $V_{fg} < 0$ V. $V_i = V_e = V_g = 6$ V, $V_d = 1.02$ V, $V_f = 1.26$ V.

Fig. 3. Voltage waveforms of the proposed ESD detection circuit under the ESD stress event.

Under normal operating conditions, the spectre-simulated results in Fig. 4 show that the voltage on node “A” (V_A) is 5.4 V (3VDD). V_i , V_d and V_B are 3.6 V (2VDD). V_e , V_f and V_C are 1.8 V (VDD). All of the transistors in the proposed circuit are protected out of gate-oxide reliability issues. V_g is 104 mV. The enhanced path is kept in off state. The leakage current of the proposed circuit is only 2.8 nA at 27°C and 243 nA at 120°C. The specific dimensions of this circuit are shown in Table I. This proposal ESD circuit is aimed to meet HBM-4 kV (Human Body Mode).

Fig. 4. Voltage waveforms and the leakage current of the proposed circuit under normal circuit operating conditions.

Table I. Dimensions of devices of the proposed circuit

Devices	MP0/1/2	MN0	MN4/5/6	MN1/2/3
W/L ($\mu\text{m}/\mu\text{m}$)	150/0.15	5/0.15	50/0.15	20/0.150
Devices	MP5/6/7	MP3/4	R1	C0
W/L ($\mu\text{m}/\mu\text{m}$)	50/0.15	1/1	150 k Ω	2 $\mu\text{m}/1 \mu\text{m}$, M = 130

4.2 Monte Carlo simulation

Monte Carlo simulations are performed using the industry compatible SMIC 28-nm HKMG model parameters. Accomplished in process & mismatch analysis, three times standard deviation (3σ) is used as the variances of parameters and mismatch of MOS and resistor. In this MC simulation, 4000 trials were run as shown in Fig. 5. Under ESD conditions, the trigger current is 31.6 mA in the worst case; and the trigger current can reach 42.7 mA in the best case.

4.3 Immunity to power supply noise

A typical power supply noise of 5~10% is considered for such analysis [12]. In this circuit, the power supply noise is set to be a sinusoidal signal with a wide frequency range starting with DC up to 1 GHz and amplitude of 500 mV from VDD to VSS. In Fig. 6, the simulating result of this proposed design under the 1 GHz power

Fig. 5. Monte Carlo simulations of the proposed circuit in 28 nm HKMG CMOS process

supply noise shows that the current at trigger node stays below $5\mu\text{A}$ and the voltage stays below $500\mu\text{V}$; as a result, the circuit is robust against the power supply noise.

Fig. 6. The voltage and current response of our proposed circuit to the 1 GHz power supply noise

5 Discussion

In this section, the comparison between the proposed detection circuit and the four prior detection circuits mentioned in section 2 is shown in Table II. This proposed circuit is realized in an advanced CMOS process with only one capacitor and low leakage current.

The leakage current of our proposed circuit is relatively low. Unlike the bias circuits in Ref. [1] which generate large leakage currents, the bias circuit in our proposed design applying three gate-to-source connected NMOS transistors can keep a very low leakage current.

The trigger current of our proposed circuit is 36.4 mA in 28 nm HKMG CMOS process. To compare the performance in a same standard, the referenced circuits are also applied in the 28 nm HKMG CMOS process. Their trigger currents are

Table II. Performance summary and comparison

	Proposed	Circuit A in Ref. [1]	Circuit B in Ref. [1]	Circuit A in Ref. [9]	Circuit B in Ref. [9]
Technology	28 nm HKMG	130 nm	130 nm	180 nm	90 nm
Power supply (V)	1.8	1.2	1.2	1.8	1.2
3VDD (V)	5.4	3.3	3.3	5	3.6
ESD-like voltage (V)	6	6	6	5	5
Trigger transistor W/L ($\mu\text{m}/\mu\text{m}$)	150/0.15	N/A	N/A	150/0.18	100/0.12
Capacitor number	1	2	1	3	6
Trigger current (mA)	36.4	35	48	36	38
I_{leak} (detection circuit) @27°C (nA)	2.8	N/A	N/A	0.9	200

3.85 mA, 25.6 mA, 35.9 mA and 34.2 mA, respectively. Therefore, the trigger current of our proposed circuit is enhanced 89.4%, 29.7%, 1.4% and 6%, respectively, compared with the other four referenced circuits.

The layout area of the proposed circuit is relatively small. The layout diagram of our proposed circuit is shown in Fig. 7. As a common sense, the capacitor occupies larger layout area than other devices in the ESD detection circuit. In Table II, we compared the capacitor number of these circuits. Our proposed circuit only needs one capacitor.

Fig. 7. The layout diagram of our proposed detection circuit

6 Conclusion

In this paper, a novel high performance $3\times VDD$ -tolerant ESD detection circuit is proposed. This proposed circuit has a high trigger current by adding an additional control sub-path and an enhanced path. It can still maintain low leakage current and small layout area. The simulation results in 28 nm 1.8 V HKMG CMOS process show that its trigger currents can reach 36.4 mA and the leakage current is only 2.8 nA at 27°C with only one capacitor in this design.

Acknowledgments

This work is supported by the “Strategic Priority Research Program” of the Chinese Academy of Sciences (XDA09020402), National Integrate Circuit Research Program of China (2009ZX02023-003), National Natural Science Foundation of China (61376006, 61401444, 61504157, 61622408), Science and Technology Council of Shanghai (14ZR1447500, 15DZ2270900).