An improved phase digitization mechanism for fast-locking low-power all-digital PLLs

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Abstract: An improved phase digitization mechanism is designed to overcome limited lock-in range of low-power all-digital phase-locked loop (ADPLL) with phase prediction and edge snapshot circuit. The proposed mechanism including a dual-mode multiplexer-based time-to-digital converter (TDC) and accessional algorithm is verified in a modelled and simulated ADPLL. Results show that the ADPLL is able to lock in 7.8 μ s, i.e., 187 cycles with a 24 MHz reference clock. The ADPLL also has strong recovery capability from sudden disturbance, for instance, it recovers in 8 μ s with 0.38% disturbance.

Keywords: ADPLL, TDC, fast locking, low power, phase digitization

Classification: Integrated circuits

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1 Introduction

Phase-locked loops (PLLs) are widely used as local oscillator (LO) generator in transceivers and consume a significant share of the total power. All-digital phase-locked loops (ADPLLs) [1, 2, 3, 4, 5, 6] are preferred in nanoscale CMOS with the merits of lower cost, power consumption, area and shorter locking time comparing to analog PLLs [7, 8]. In a counter-assisted ADPLL [1, 2, 3, 4, 5], time-to-digital converter (TDC) is employed as fractional phase detector and measures edge time difference between the high-frequency output clock CKV and reference clock $FREF$. The TDC quantization of timing estimation which dominates the loop's in-band phase noise at the ADPLL output could be minimized by improving the TDC timing resolution. The resolution of conventional delay-line-based TDC is proportional to one inverter delay. Vernier TDC uses the difference between two delay lines as resolution to realize lower phase noise with quadratic relationship; for instance, a 90% resolution decrease from 60 ps to 6 ps leads to 99% decrease (-20 dBc/Hz) in phase noise. But it consumes much power while covering and working at full digital-controlled oscillator (DCO) output clock CKV because an excessive number of stages are required. Phase prediction based on digital-to-time converter (DTC) [3, 4, 5] and edge snapshot circuit [4, 5] have been used to reduce the power consumption of Vernier TDC.

As shown in Fig. 1, the reference clock is delayed using a DTC according to estimated next time difference. The delayed reference clock is approximately synchronized with the CKV edges when the loop is locked such that required TDC timing range could be narrowed. Edge snapshot circuit reduces input clock rate by catching one necessary edge of high-frequency CKV to further reduce power consumption. If two methods are used together, much power consumption is saved. Unfortunately, fractional phase error is hard to be detected when it is outside narrowed TDC's range. During initial tuning processes, if narrow bandwidth is set,

Fig. 1. ADPLL architecture with phase prediction, edge snapshot circuit and proposed DTC offset block.

accumulated phase error with slow adjustment may cause out-of-range issues. In practice, sudden disturbance such as environment change or supply fluctuation may also cause rapid change of phase error which is easily out of TDC's range [6]. To solve this out-of-range problem, an improved phase digitization mechanism including a dual-mode multiplexer-based TDC and accessional DTC offset algorithm is proposed to achieve fast locking and recovery time. The TDC switches between full-covered delay-line-based and narrowed Vernier architecture with coarse or fine resolution according to tuning processes with different phase error. The algorithm extends narrowed TDC timing range by adding a new factor *OFFSET* to DTC.

2 Dual-mode multiplexer-based TDC

Fig. 2 shows the architecture of the proposed dual-mode multiplexer-based TDC. It delays two input asynchronous clocks (*FREFDS* and *CKVS*) by different paths according to control signals (*SEL_TDC* and *EN*) in different tuning processes such that coarse-mode and fine-mode TDC can be formed with different resolution.

Fig. 2. Proposed dual-mode multiplexer-based TDC.

EN is the main switch signal of the TDC. When $EN = 1$, TDC is off for power saving. When $EN = 0$, TDC starts working. SEL_TDC determines which mode is chosen. In both modes, $FREFDS$ is delayed by a delay line with resolution of t_{mux0} and sent to registers' Clk ports, where t_{mux0} is the delay time value of a multiplexer from input 0 to output. The registers are sense-amplifier-based D-type flip-flops (SA-DFF) with very small setup and hold windows to avoid metastability problems [9].

In coarse mode, SEL_TDC is set to be 0. $CKVS$ is delayed by t_{mux0} as input D of the array of registers. The coarse resolution is t_{mux0} . The number of multiplexers N is limited by the need to cover full DCO output period:

$$N \geq \frac{\max(T_V)}{\min(t_{mux0})} := N_1 \quad (1)$$

In fine mode, SEL_TDC is set to be 1. $CKVS$ is delayed by a delay line with resolution of t_{mux1} and sent to registers' D ports, where t_{mux1} is the delay time value of a multiplexer from input 1 to output. The resolution of fine mode is $t_{mux0} - t_{mux1}$. N stages cover one or more DTC step Δt_{dte} , which requires:

$$N \geq \frac{\max(\Delta t_{dte})}{\min(t_{mux0} - t_{mux1})} := N_2 \quad (2)$$

A little more stages than N_2 can help improve frequency capture capability. But too many cells lead to complex circuit with more unnecessary power consumption. Usually, $2N_2$ is a good choice if $2N_2 \geq N_1$ is already satisfied. In this condition, redundant $N - N_1$ stages should be off to save power in coarse mode as shown in right part of Fig. 2. If $2N_2 \leq N_1$, N is set as N_1 . All stages are the same as those in left part.

TDC nonlinearity and inaccurate TDC scaling factor caused by process, voltage and temperature (PVT) variations are sources of fractional spurs by creating a repeated phase error [10]. In conventional delay-line-based TDC, the TDC nonlinearity is almost entirely dominated by the even-odd timing mismatch of inverters which does not exist in the proposed multiplexer-based TDC. In the other hand, the TDC scaling factor can be compensated by period normalization. Spurs also can be diminished by loop filters.

3 DTC offset algorithm

Fig. 3 shows the signal flow of tuning processes including proposed DTC offset algorithm. At first, integral phase error $\phi_{e,i}$ is calculated by counters without considering fractional part:

$$\phi_{e,i} = R_{R,i} - R_V \quad (3)$$

where $R_{R,i}$ and R_V are estimated integral reference phase and variable phase. Coarse-mode TDC is off until average differential phase error is within DCO coarse step $\Delta\phi_{DCO,c}$.

Fig. 3. Signal flow of tuning processes including proposed DTC offset algorithm.

In coarse mode, fractional phase error $\phi_{e,f}$ is measured with a coarse time quantization resolution t_{mux0} :

$$\phi_{e,f} = \frac{TDC_{NUM}}{K_{TDC,c}} - DTC_{REM} \quad (4)$$

where TDC_{NUM} is the position of the transition detected from 0 to 1 in TDC output $Q[0:N-1]$, $K_{TDC,c} = T_V/t_{mux0}$ is normalized coarse TDC gain, T_V is the period of CKV and DTC_{REM} is DTC quantification phase error.

Then TDC is switched to fine mode with a fine time resolution of $t_{mux0} - t_{mux1}$ if differential phase error including integral and coarse fractional parts is within DCO fine step $\Delta\phi_{DCO,f}$.

In fine mode, $\Sigma\Delta$ modulator is used as a time-averaged dithering mechanism to further increase frequency resolution [11]. As integral phase error becomes zero, counters are off to save power.

The proposed DTC offset algorithm takes effect during the fine mode. It adds a new factor *OFFSET* to DTC according to TDC states: *IN* and *OUT* (including *OUTUP* and *OUTDOWN*). *IN* means phase error is within TDC range while *OUTUP* means that the number of TDC stages N is not enough and outputs of registers in TDC are all 0. On the other hand, *OUTDOWN* means $CKVS$ leads $FREFDS$ which is usually invisible in this architecture because snapshot circuit catches the next CKV rising edge after $FREFD$ rising edge and the negative phase error becomes positive value periodically with negative integral carry. Unfortunately, counters are already off and the radical change of fractional phase error increases locking time. Two buffers in Fig. 1 are added to change negative snapshot capture range from $(0, T_V)$ to $(-D, T_V - D)$ where D is the delay time of buffers. Thus slightly negative phase error can be remained between $FREFDS$ and $CKVS$ which is state *OUTDOWN*. In *OUTDOWN* state, the outputs of registers in TDC are all 1.

Assuming that frequency error is already very small during this mode and phase error is adjusted gradually, adding *OFFSET* to DTC code DTC_{NUM} can move TDC range with step of $K_{DTC} = T_V/\Delta t_{dtc}$ which is normalized DTC gain as Fig. 4 shows. For example, if the original TDC phase-detect range $(0, N/K_{TDC,f})$ in Fig. 4a is not enough, *OFFSET* = 1 could delay $FREFDS$ by one more DTC cell, which means move TDC range to $(1/K_{DTC}, 1/K_{DTC} + N/K_{TDC,f})$ as shown in Fig. 4b. The adder is implemented in modulo arithmetic in order to practically limit the length of DTC stages and avoid negative DTC code:

Fig. 4. Diagram of phase digitization mechanism (a) without proposed DTC offset algorithm and (b) with proposed DTC offset algorithm.

$$DTC_{NUM}' = \text{mod}(DTC_{NUM} + OFFSET, K_{DTC}) \quad (5)$$

And the phase error is expressed as:

$$\phi_{e,f} = \frac{TDC_{NUM}}{K_{TDC,f}} + \frac{OFFSET}{K_{DTC}} - DTC_{REM} \quad (6)$$

where $K_{TDC,f} = T_V/(t_{mux0} - t_{mux1})$ is normalized fine TDC gain. The momentary out-of-range phase error is estimated by previous values:

$$\phi_{e,f}[k] = 2\phi_{e,f}[k-1] - \phi_{e,f}[k-2] \quad (7)$$

If *OFFSET* cannot help for C ($= 2$ in this design) periods, which means a big disturbance, it's better to go back to process with counters and coarse-mode TDC. In this algorithm, fast-locking processes are achieved by using two modes of TDC flexibly and avoiding long-time out-of-range states.

4 Implementation and simulation results

To show the effectiveness of the proposed mechanism, a dual-mode TDC is simulated by HSPICE in 180 nm technology first. It uses a 24 MHz frequency reference clock *FREF* and a high-speed clock *CKV* generated by DCO with frequency of 300–1300 MHz. Results show that coarse and fine resolution are 108.8 ps and 4.5 ps. So $N = 64$ and $N_1 = 32$ are chosen. The total power consumption of the dual-mode TDC, DTC and edge snapshot circuit is only 638 μ W. The nonlinearity of this TDC is from device mismatches and signal couplings which is invisible in simulation results. Therefore, the simulated differential nonlinearity (DNL) and integral nonlinearity (INL) are almost zero. The propagation delay of the SA-DFF with near-zero setup time and hold time is 170 ps, which is normal in this technology.

Then an ADPLL is modelled and simulated by Verilog code. Fig. 5a shows an example of initial locking processes with target frequency at 403.05 MHz (channel 3 in IEEE 802.15.6) from an initial lowest 300 MHz. The entire locking processes including integral, coarse and fine modes take about 7.8 μ s. Fig. 5b shows the locking time with different target frequency. The locking time fluctuates because it takes shorter time if the target frequency is closer to the initial value in either coarse or fine mode. The average and maximum locking time are 8 μ s and 10 μ s.

Fig. 5. (a) Initial locking processes example with target frequency at 403.05 MHz from 300 MHz; (b) Simulated locking time with different target frequency.

In an ADPLL, the internal phase noise sources are mainly from quantization effects including TDC noise and DCO noise with $\sum \Delta$ noise shaping. The simulated peak-to-peak and root mean square (rms) jitter of the example showed in Fig. 5a are 0.61 ps and 1.13 ps when DCO resolution is set as 0.313 ps according to a real DCO and MASH 1-1-1 $\sum \Delta$ modulator is used. In real condition, outside noise sources would make measured jitter a little bigger than the simulated value. To verify the effectiveness of proposed phase digitization mechanism with various DCO resolutions, Fig. 6 shows the peak-to-peak jitter, rms jitter and locking time.

Fig. 6. (a) Simulated peak-to-peak jitter, rms jitter and (b) locking time with different DCO resolutions

In the same simulation environment without proposed mechanism, as Fig. 7a shows, the initial locking time is as long as 55 μs because of intermittent out-of-range issues. Even a small disturbance can cause unrecoverable error. Proposed mechanism not only takes effect in initial locking processes, but also improves recovery ability from disturbance. A momentary phase disturbance is usually from reference clock and clock paths. As Fig. 7b shows, ADPLL recovers in 4–7 μs according to different phase disturbance from 1.61% to 12.1%. Frequency disturbance from DCO is more serious which can cause sustained phase disturbance. When a slight 0.05% frequency disturbance occurs, as Fig. 7c and Fig. 7d shows, ADPLL finds new DCO control codes related to accumulated phase error and recovers rapidly in 5 μs with DTC offset algorithm. If the frequency disturbance is as great as 0.38%, as shown in Fig. 7e and Fig. 7f, ADPLL recovers in 8 μs by converting TDC mode when DTC offset algorithm is ineffective.

The comparison table is shown in Table I. [4, 5] and this work are all based on the low-power architecture with DTC phase prediction and edge snapshot circuit while [3] uses only the first one. [3, 4] are hard to achieve fast locking time only by the integer phase path because of limited TDC range. In this work, the results of the ADPLL without proposed mechanism is used to simulate this condition for fair comparison with same loop filters, frequency and TDC/DCO modules. Results show that it takes longer locking time and is unable to recover from even a small disturbance. [5] presents a digital phase unwrap and achieves recovery ability from disturbance. The proposed mechanism achieves different recovery time according to different disturbance strength, which are both shorter than [5].

Fig. 7. (a) Initial locking processes without proposed mechanism. (b) Phase error recovery from various phase disturbances. (c) Normalized frequency deviation and (d) accumulated phase error when 0.05% frequency disturbance occurs. (e) Normalized frequency deviation and (f) accumulated phase error when 0.38% frequency disturbance occurs.

Table I. Locking time and recovery capability comparison

	[3]	[4]	[5]	This work		
				w/o proposed mechanism	w/i proposed mechanism	
Architecture	DTC+TDC ADPLL	DTC+TDC +snapshot ADPLL	DTC+TDC +snapshot ADPLL	DTC+TDC +snapshot ADPLL		
Reference (MHz)	26	32	N/A	24	24	
Locking time (μs)	70	20	N/A	55	7.8	
Locking time (cycles)	1820	640	N/A	1320	187	
Disturbance (%)	N/A	N/A	0.3	0.05	0.05	0.38
Recovery time (μs)	N/A	N/A	11	unrecoverable	5	8
RMS jitter (ps)	N/A	1.7	1.98	0.61		
Experimental results types	Simulated	Measured	Measured	Simulated		

5 Conclusion

The improved phase digitization mechanism is effective for low-power ADPLL architecture with phase prediction and edge snapshot circuit. The proposed mechanism including a dual-mode multiplexer-based TDC and accessional algorithm overcomes its limited lock-in range and achieves fast locking and recovery time.

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