A PMOS read-port 8T SRAM cell with optimized leakage power and enhanced performance

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Abstract: This paper presents a novel PMOS read-port 8T SRAM cell, in which the read circuit is constructed by two cascaded PMOS transistors, and hence the leakage power is significantly optimized compared to the conventional 8T cell. Meanwhile, it also exhibits high area efficiency due to an equalized quantity of NMOS and PMOS transistors per cell. Furthermore, the proposed cell has sufficient potential to enhance performance by employing a Half-Schmitt inverter. The measurements indicate that the proposed cell outmatches conventional 8T cell in terms of leakage suppression and area saving, thus making it a superior choice for ultra low power applications.

Keywords: SRAM, 8T cell, leakage power, low power

Classification: Integrated circuits

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1 Introduction

With the booming of low power applications in recent years, power consumption rather than performance becomes a major design concern [1]. SRAM dominates total chip power especially leakage power, thus the low leakage SRAM is urgently needed [2]. Near and sub-threshold SRAM is effective to reduce power dissipation, so they are extensively used in low power applications [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15]. 8T SRAM cell has taken the place of 6T cell to be a popular choice for the near and sub-threshold operation [2, 3, 4, 5, 6, 7]. Unfortunately, 8T cell has additional leakage path compared to 6T cell, thus increasing the cell leakage [8]. In addition, the I_{ON}/I_{OFF} ratio decreases in the near and sub-threshold region, which even incurs a wrong read operation. Therefore, peripheral assistant technology like virtual ground is proposed to alleviate the problem [9, 10, 11, 12, 13]. However, it not only takes circuit penalty but also results in corresponding power consumption [14].

This paper proposes a novel 8T cell, and the contributions of this work can be summarized as follows: 1. This cell can essentially economize leakage power without additional peripheral circuit; 2. The read mechanism of the cell offers

potential to promote the sacrificed performance; 3. The cell has a balanced amount of PMOS and NMOS transistors, which leads to area reduction. To our knowledge, it is the first PMOS read-port SRAM operating in the low voltage region.

Unlike 6T cell, conventional 8T cell (C8T cell) has an isolated read port which is formed by two stacked NMOS transistors (N5, N6), as shown in Fig. 1(a). It facilitates a successful read operation in low supply condition, but induces extra leakage current. In contrast, the read port in our cell is constituted by two stacked PMOS transistors (P3, P4) to suppress the leakage current, as shown in Fig. 1(b). Therefore, a pre-discharge read mechanism instead of a conventional pre-charge mechanism is applied in our cell. To perform a read operation, read bitlines (RBLs) in C8T cell and our cell are initialized to “1” and “0”, respectively. In Fig. 1(a), the read operation is a discharging process through N6 and N5 when $QB = 1$, while in Fig. 1(b), it is a charging process through P3 and P4 when $QB = 0$. The charging process benefits the read performance, which will be described in the following analysis. Besides, write and hold operations are similar between two cells.

In addition, multi-threshold technology is popularly used to construct a SRAM cell in order to guarantee high read performance and low leakage power consumption [16]. Hence, SVT (Standard Threshold Voltage) transistors are employed for read port to enhance read performance and HVT (High Threshold Voltage) transistors are employed for the 6T part to suppress leakage current. As a result, the read port contributes a significant part of total cell leakage. Thus, reducing the leakage of the read port is becoming important.

Fig. 1. Two cells (a) Conventional 8T cell (b) Proposed PMOS 8T cell

2 Leakage power optimization

A leakage current gap exists between PMOS and NMOS transistors since PMOS is substantially weaker than NMOS, and it becomes even larger when the transistors are cascaded. Thus, our read port consumes much less leakage power than the C8T read port. In order to do the evaluation accurately, NMOS transistor is assumed to have the V_{th} stand deviation of 20 mV while PMOS transistor is assumed to have that of 16 mV. Fig. 2 illustrates the leakage power of our cell and C8T cell at different voltages and temperatures. 10000 Monte Carlo simulations are executed at each voltage and temperature, and the final leakage value is an average of these 10000 results. Clearly, our cell (PMOS 8T cell) consumes less leakage power at all conditions comparing with C8T cell. The related leakage power reduction ratio between C8T cell and our cell is shown in Fig. 3. At the same temperature, our cell behaves competitively in leakage reduction as the voltage drops. Meanwhile, at the same voltage, along with the reduction of temperature, the ratio increases at first to

reach a maximum value and then switches to decrease. The switching point varies at different voltages and becomes closer to ‘0’ when the voltage gets lower. This phenomenon appears because temperature affects transistor current differently at various voltages. In the super-threshold region, the current decreases as the temperature increases, while it is reverse in the low voltage region. Hence, the variation of switching point is a combined effect of temperature and voltage. The ratio arrives at 2.6X at the best case and revolves around 2X at most cases, which is a gratifying result in leakage optimization. And fortunately, even at the worst case, leakage reduction could still be achieved (1.4X). Moreover, the relative deviation (σ/u) of 10000 values of our cell in each simulation point is better than that of the C8T cell, which indicates our cell leakage variation is suppressed. Overall, the suppressions of leakage value and variation both overwhelm that of C8T cell. So, our read bitline sensing margin is extended, which enhances the cell stability.

Fig. 2. Static power consumed by conventional 8T and our cell

Fig. 3. Leakage optimization ratio

3 Promotion of aggravated performance

On the other hand, read performance of our cell is compromised due to the weak drive-ability of the stacked PMOS transistors. Although it could be tolerated because low power chips prioritize power consumption over performance [1, 8], we still utilize our read mechanism to promote the sacrificed performance.

Typical organizations for C8T SRAM and our SRAM are shown in Fig. 4, where 256 cells are connected to a bitline. The figure models two worst read performance scenarios for C8T cell and our cell, respectively. In C8T organization, the worst scene happens when the selected cell is “0” ($Q = 0$, $QB = 1$) and the unselected cells are “1” ($Q = 1$, $QB = 0$), which minimizes the pull down reading current. As for our organization, the worst situation comes out when the selected cell is “1” ($Q = 1$, $QB = 0$) and the unselected cells are “0” ($Q = 0$, $QB = 1$). Since 256 cells introduce large capacitance, it needs considerable latency to change the bitline state. Unfortunately, our pull up current is not as strong as the conventional pull down current, so our read performance is exacerbated.

Fig. 4. Worst read performance scenarios (a) Worst scenario for conventional 8T cell (b) Worst scenario for proposed 8T cell

In order to mitigate the aggravation of performance, the characteristic of transistors and our read mechanism can be utilized. The drive-ability gap between NMOS and PMOS transistors enlarges along with the scaling of supply voltage. Therefore, the voltage transfer curve (VTC) of the inverter lies easily towards “0” especially in low supply condition. When an inverter is connected to the read bitline, the charging process will be quickly sensed by the inverter due to the skewed VTC. Consequently, instead of charging to the nominal supply voltage level to represent “1”, RBL can just charge to the level which activates the inverter. Hence, adding an inverter into our organization improves the aggravated performance. Furthermore, a Half-Schmitt (HS) inverter is designed to shift its switching threshold to “0” by adding two PMOS transistors (P2, P3) into the normal structure, as shown in Fig. 5(a). This modification not only strengthens the pull down path to skew the switching threshold closer to ‘0’, but also steepens VTC, as shown in Fig. 5(b). Hence, performance can be further enhanced by adopting a HS inverter into our bitline with neglected area overhead. We quantify performance by the metric of latency, and the simulation result is shown in Fig. 6. Original PMOS 8T stands for our original organization without an inverter, while Schmitt PMOS 8T stands for the organization with a HS inverter. Analyzed from the figure where the latency of Schmitt PMOS 8T SRAM is normalized to 1, read performance is

significantly enhanced by applying the HS inverter, especially in the low voltage region.

Fig. 5. Half-Schmitt inverter (a) Schematic (b) VTCs of HS inverter and normal inverter

Fig. 6. Improvement ratio between PMOS and Schmitt 8T SRAM

When read scene changes to the situation where the selected cell is “0” ($Q = 0$, $QB = 1$) and the unselected cells are “1” ($Q = 1$, $QB = 0$), the employment of the HS inverter reduces this read margin compared with our original organization without the inverter, but it is still better than C8T cell. Fig. 7 shows the worst read margin scenarios for our cell and C8T cell, respectively. Total leakage occupied by our unselected cells is much less than that of C8T cell, which gives our bitline abundant noise margin. Thus, the sacrifice of our bitline noise margin could be tolerated compared with the C8T cell.

In addition, 10000 Monte Carlo simulations are run for our PMOS read port and conventional NMOS read port, and the result is shown in Fig. 8. It indicates that our I_{ON}/I_{OFF} ratio is much better than that of C8T cell. So a stronger static keeper could be employed to compensate the leakage current of the unselected cells to make our bitline more stable, as shown in Fig. 7. Furthermore, it does not weaken the read performance due to the wide gap between the I_{ON} and I_{OFF} current.

4 High area efficiency

The SRAM was fabricated in 130 nm, 1P8M CMOS technology. The combination of 6 NMOS transistors and 2 PMOS transistors in C8T cell requires two n-well boundaries to acquire a streamlined layout, which induces area penalty [17]. Instead, our cell has 4 NMOS and 4 PMOS transistors, which achieves a smooth

Fig. 7. Worst read noise margin scenarios (a) Worst scenario for conventional 8T cell (b) Worst scenario for proposed 8T cell

Fig. 8. I_{ON}/I_{OFF} ratio between PMOS read port and NMOS read port

layout with only one n-well boundary. At the same time, in order to promote the cell stability in the low voltage region, we also apply reverse short channel effect in the PMOS transistors [3]. Hence, 2X longer channel length is employed in the PMOS transistors, as shown in Fig. 9. Finally, our area consumption is saved by about 10% compared to C8T cell. Furthermore, the area optimization is expected to be obtained for other process technologies and normal channel length, thus making our cell a general solution.

5 Experiment result

A 6 Kb 130 nm test chip was fabricated to demonstrate our ideas. The layout and die photo of the chip are shown in Fig. 10. We also fabricated a 6 Kb C8T SRAM for leakage power and performance comparison.

Fig. 9. Layout (a) C8T cell (b) Proposed 8T cell

Fig. 10. Photos (a) Layout (b) Die

Our SRAM could function from 1.2 V down to 0.35 V at room temperature. Furthermore, due to the employment of HS structure in the bitline, the highest frequency of our SRAM at each voltage is just a little compromised compared to the C8T SRAM, as shown in Fig. 11. In contrast, our SRAM shows 1.8X lower leakage power consumption compared to the C8T SRAM, as shown in Fig. 12.

Fig. 11. Performance comparison

Fig. 12. Leakage power comparison

6 Conclusion

This paper proposes a PMOS read-port 8T cell for optimizing leakage power, the simulation and measurement results indicate that the proposed cell achieves excellent leakage and area efficiency as the voltage drops. In addition, the aggravated performance is alleviated by incorporating the Half-Schmitt inverter. A proposed 6 Kb SRAM fabricated in a 130 nm CMOS technology obtains 1.8X reduction in leakage power dissipation and 10% reduction in area consumption compared with the conventional 8T SRAM.

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