A 0.9 V 2.72 μ W 200 kS/s SAR ADC with ladder-based time-domain comparator

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Abstract: This paper presents a 200 kS/s 12-bit successive approximation ADC with a new ladder-based time-domain comparator. The proposed comparator utilizes differential multi-ladder stages, resulting in improvement of gain and noise performance. The chip is designed and fabricated in a standard 0.18 μ m CMOS technology with area of 0.127 mm². With a supply of 0.9 V, the ADC consumes 2.72 μ W at the sampling rate of 200 kS/s. The measured SNDR and SFDR are 61.6 dB and 66.1 dB respectively, providing an ENOB of 9.9 bits, and the corresponding FOM of 28 fJ/conv-step.

Keywords: bio-medical devices, SAR ADC, time-domain comparator

Classification: Integrated circuits

References

- [1] R. F. Yazicioglu, *et al.*: “A 60 μ W 60 nV/Hz readout front-end for portable biopotential acquisition systems,” *IEEE J. Solid-State Circuits* **42** (2007) 1100 (DOI: [10.1109/JSSC.2007.894804](https://doi.org/10.1109/JSSC.2007.894804)).
- [2] R. F. Yazicioglu, *et al.*: “A 200 μ W eight-channel EEG acquisition ASIC for ambulatory EEG systems,” *IEEE J. Solid-State Circuits* **43** (2008) 3025 (DOI: [10.1109/JSSC.2008.2006462](https://doi.org/10.1109/JSSC.2008.2006462)).
- [3] D. D. He, *et al.*: “A 58 nW ECG ASIC with motion-tolerant heartbeat timing extraction for wearable cardiovascular monitoring,” *IEEE Trans. Biomed. Circuits Syst.* **9** (2015) 370 (DOI: [10.1109/TBCAS.2014.2346761](https://doi.org/10.1109/TBCAS.2014.2346761)).
- [4] N. Van Helleputte, *et al.*: “A 345 μ W multi-sensor biomedical SoC with bio-impedance, 3-channel ECG, motion artifact reduction, and integrated DSP,” *IEEE J. Solid-State Circuits* **50** (2015) 230 (DOI: [10.1109/JSSC.2014.2359962](https://doi.org/10.1109/JSSC.2014.2359962)).
- [5] M. Liu, *et al.*: “A 7.1 fJ/conv.-step 88 dB-SFDR 12 b SAR ADC with energy-efficient swap-to-reset,” *ESSCIRC Conf. 42nd European Solid-State Circuits Conf.* (2016) (DOI: [10.1109/ESSCIRC.2016.7598328](https://doi.org/10.1109/ESSCIRC.2016.7598328)).
- [6] A. Agnes, *et al.*: “A 9.4-ENOB 1 V 3.8 μ W 100 kS/s SAR ADC with time-domain comparator,” *ISSCC Dig. Tech. Papers* (2008) 246 (DOI: [10.1109/ISSCC.2008.4523149](https://doi.org/10.1109/ISSCC.2008.4523149)).
- [7] S. K. Lee, *et al.*: “A 21 fJ/Conversion-step 100 kS/s 10-bit ADC with a low-noise time-domain comparator for low-power sensor interface,” *IEEE J. Solid-State Circuits* **46** (2011) 651 (DOI: [10.1109/JSSC.2010.2102590](https://doi.org/10.1109/JSSC.2010.2102590)).
- [8] L. Deng, *et al.*: “A 12-bit 200 KS/s SAR ADC with a mixed switching scheme and integer-based split capacitor array,” *IEEE 11th International New Circuits*

- and Systems Conference (NEWCAS) (2013) (DOI: [10.1109/NEWCAS.2013.6573564](https://doi.org/10.1109/NEWCAS.2013.6573564)).
- [9] Z. Zhu, *et al.*: “A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18- μ m CMOS for medical implant devices,” IEEE Trans. Circuits Syst. I, Reg. Papers **62** (2015) 2167 (DOI: [10.1109/TCSL.2015.2451812](https://doi.org/10.1109/TCSL.2015.2451812)).
- [10] Y. Zhang, *et al.*: “A 10-b 200-kS/s 250-nA self-clocked coarse-fine SAR ADC,” IEEE Trans. Circuits Syst. II, Exp. Briefs **63** (2016) 924 (DOI: [10.1109/TCSII.2016.2538139](https://doi.org/10.1109/TCSII.2016.2538139)).

1 Introduction

Expanding demands for bio-medical devices have driven extensive research on integrated circuit technologies for micro-power SoCs. These bio-medical devices are used for detecting and processing bio-potential signals, with dynamic range from μ V to mV covering limited frequency band from sub-1 Hz to 10 kHz, as illustrated in Fig. 1. Their building blocks, including low noise amplifiers (LNA), analog-to-digital converters (ADC) and processors, should be optimized for the proper performance as well as strict energy budget for long term continuous monitoring [1, 2, 3, 4].

As a fundamental building block, the architecture, speed, resolution of the ADC should be chosen carefully based on overall system requirements, because these specifications will significantly impact on the system power consumption. Among different types of ADCs, successive approximation (SAR) ADC of 10–12 bit resolution has advantages of simple structure and low power consumption which make it the best choice in such application scenarios [5].

The most efficient way to reduce power consumption, especially for the digital circuits, is to lower the supply voltage. Nevertheless, the low supply voltage makes it more difficult to design analog circuits. In this work, a ladder-based time domain comparator is proposed which works efficiently under sub-1 V supply voltage. Instead of operating in voltage-domain, it transforms voltage difference into delay difference then gives the result by comparing the duration. Therefore, it is suitable for low-voltage application and compatible with sub-micro CMOS technology. Moreover, digital circuits are also optimized to reduce the extra dynamic power.

Fig. 1. Frequency and amplitude characteristics of bio-potential signals [1]

Fig. 2. (a) SAR ADC architecture; (b) Flow chart of the proposed ADC

2 Architecture

Fig. 2(a) shows the block diagram of the proposed 12-bit low power SAR ADC, consisting of a differential capacitive-DAC array (CDAC), a ladder-based time-domain comparator and control logic block for successive approximation. The flow chart in Fig. 2(b) depicts the successive approximation procedure. At the sampling phase, the differential input signal is sampled at the output of the CDAC and all the bottom plates are reset to the common-mode voltage V_{CM} . At the conversion phase, the comparator performs the first comparison directly. Next, the differential outputs of CDAC, V_+ and V_- are added or subtracted a binary-weight voltage, $V_{REF}/2^{i+1}$, according to the comparator output. Differently for the last step, only one capacitor C_{11} is switched from V_{CM} to GND as a monotonic switching procedure.

3 Ladder-based time-domain comparator

Fig. 3 shows the fundamental blocks of time-domain comparator which consists of two voltage-to-time converters and a binary phase detector [6, 7]. The voltage-to-time converter usually consists of multi-stage voltage control delay lines (VCDLs) where the delay time is proportional to the value of the input voltage. For the binary phase detector, a flip-flop or a dynamic RS latch are conventionally used due to their simplicity and fast latch operation.

3.1 Design principle

This paper proposed a new ladder-based time-domain comparator (LB TDC) consisting of ladder-based VCDLs and a binary phase detector. As Fig. 4 shown, transistors M1 and M2 are stacked together to control the delay time and M3 and M4 are used to pull up node B and C to VDD when comparator is disable. The delay time from node A to B is proportional to the difference of the gate-source voltage V_{GS} and threshold voltage V_{TH} . When V_{GS} approaches to V_{TH} , M1 starts to conduct which makes node B discharge from VDD to GND. Thus, if setting the input voltage V_{IN} around the V_{TH} , node B starts to discharge only when the voltage in node A approaches to GND as shown in Fig. 4(b). Therefore, the proposed ladder-based VCDL can make full use of delay time from node to node.

3.2 Gain and noise for the ladder-based VCDL

As the differential input of the comparator becomes smaller, the transistor operates in sub-threshold region. Therefore, the delay line can be regarded as a current-starved delay model. Thus, the mathematical relation between delay time and voltage can be derived as:

$$t_d = \alpha \cdot \frac{V_{DD}}{SR} = \alpha \cdot \frac{C_L V_{DD}}{I_{SS}} \quad (1)$$

where C_L is the output load capacitor of delay line, I_{SS} is the discharging current flowing through the transistor, α is the factor of voltage-to-time conversion efficiency. In this paper, α is 1 which is twice as much as that in work [7]. Hence, the voltage-to-time gain ($\Delta t_d / \Delta V_{IN}$) can be expressed as:

$$A_{VT} = \alpha \cdot \frac{C_L V_{DD} g_m}{I_{SS}^2} = \alpha \cdot \frac{C_L V_{DD}}{\zeta V_T I_{SS}} \quad (2)$$

where I_{SS} equals to $I_{S0} e^{\frac{V_{GS}-V_{TH}}{\zeta V_T}}$, ζ is a nonlinearity factor and $V_T = kT/q$.

Fig. 3. Time-domain comparator diagram

Fig. 4. (a) Circuit of the ladder-based VCDL; (b) its timing diagram

Considering thermal noise, it manifests as time jitter at the output of each delay line, as the broken line shown in Fig. 4. Therefore, according to the Eq. 1, the value of jitter can be expressed as:

$$\overline{\Delta t_d} = \frac{\overline{\Delta V_n} C_L}{I_{SS}} \quad (3)$$

where $\overline{\Delta V_n}$ is the noise voltage at the output of the delay line.

As the LB-VCDL stacks together, V_{GS} decreases due to the voltage drop-off from the preceding stage, the delay time increases exponentially as the current $I_{SS} \propto e^{V_{GS}-V_{TH}}$. Herein, too much stacked stages will finally limit the conversion speed of the ADC. In addition, transistor working in subthreshold region suffers from bad noise performance.

For multi-stage LB-VCDL, the gain and noise can be rewrite as

$$A_{VT,N} = \frac{C_L V_{DD}}{\zeta V_T} \cdot \left(\frac{\alpha_1}{I_{SS,1}} + \frac{\alpha_2}{I_{SS,2}} + \dots + \frac{\alpha_N}{I_{SS,N}} \right) \quad (4)$$

$$\overline{\Delta t_d} = \overline{\Delta V_n} C_L \cdot \sqrt{\left(\frac{1}{I_{SS,1}} \right)^2 + \left(\frac{1}{I_{SS,2}} \right)^2 + \dots + \left(\frac{1}{I_{SS,N}} \right)^2} \quad (5)$$

where N is the stages of LB-VCDL. So the input-referred noise $\overline{\Delta V_{n,in}}$ can be calculated by $\overline{\Delta t_d}/A_{VT,N}$

$$\overline{\Delta V_{n,in}} = \kappa \cdot \frac{\sqrt{1 + e^{\frac{2V_{DS2}}{\zeta V_T}} + \dots + e^{\frac{2V_{DS,N}}{\zeta V_T}}}}{\alpha_1 + \alpha_2 e^{\frac{V_{DS2}}{\zeta V_T}} + \dots + \alpha_N e^{\frac{V_{DS,N}}{\zeta V_T}}} \quad (6)$$

where κ equals to $\frac{\overline{\Delta V_n} \zeta V_T}{V_{DD}}$ and $V_{DS,i}$ is the i-th drain-source voltage of the transistor.

Fig. 5 shows the noise comparison between the time-domain comparator in [7] and proposed one. Therefore, in order to achieve best noise performance, three-stage VCDLs (one-stage VCDL + two-stage LB-VCDL) are selected to amplify the voltage difference.

4 Implementation of other key building blocks

4.1 Capacitive-DAC array

The proposed ADC employs a integer-based split capacitor array with high 9 bits and lower 3 bits. The unit capacitor is composed by a two serial minimum MIM capacitors provided by the PDK (17.2 fF with $5 \mu\text{m} \times 5 \mu\text{m}$). The switching strategy follows a mixed switching fashion proposed in [8] to save both area and power consumption.

Fig. 5. (a) Circuit of the proposed LB TDC and (b) noise comparison with the TDC in [7]

4.2 SAR control logic

For low power SAR ADC with low sampling rate, synchronous operation is often used. Therefore, the proposed SAR ADC utilizes a synchronous SAR control logic shown in Fig. 6. It consists of a 12-bit shift register and 12 D-flip flops, which generates the sample clock and the control signals for the CDAC. By using extra logic gates, named clock-gating technique, the dynamic power is dramatically reduced because only one DFF is enabled in each clock cycle. Since a 3.2 MHz system clock has been used, the sampling rate of 200 kS/s with duty cycle of 25% is generated by the SAR control logic.

Fig. 6. Circuit of the SAR control logic

5 Measurement result

A microphotograph of the prototype ADC fabricated in UMC 0.18 μ m CMOS process is shown in Fig. 7(a), and the measurement setup is shown in Fig. 7(b). The total active area is 550 μ m $\times$ 330 μ m, with a total die size of 1.15 mm $\times$ 1.15 mm.

With the clock frequency of 3.2 MHz, maximum sampling rate of 200 kS/s is achieved. With power supply of 0.9 V, power consumption is 2.72 μ W, including 51%, 13%, 18%, 2% and 16% from the comparator, CDAC, SAR, S/H and drivers, respectively.

The SNDR and SFDR of ADC are measured using an input tone with frequency of 3.053 kHz and magnitude of -0.2 dBFS. The spectrum analysis is

Fig. 7. (a) Microphotography of the ADC prototype; (b) Measurement setup

shown in Fig. 8, which reveals the ADC achieved SNDR of 61.6 dB and SFDR of 66.1 dB, providing an effective number of bits (ENOB) of 9.9 bits. The differential nonlinearity (DNL) and integral nonlinearity (INL) of the designed ADC are shown in Fig. 9. The peak DNL and INL are +1.3/−0.96 LSB and +4.9/−2.5 LSB, respectively. In terms of the spectrum analysis, the mismatch among CDAC elements as well as the parasitic capacitance induced by the process variation and layout routing might be responsible for the large distortion. The corresponding figure-of-merit (FOM) can be derived by

$$FOM = \frac{Power}{2^{ENOB} \cdot f_s} = 28 \text{ fJ/conv-step} \quad (7)$$

Table I is the summarized performance which shows a comparable result to the state-of-art low power SAR ADCs with similar technologies.

Fig. 8. Microphotography of the ADC prototype

Fig. 9. Measured differential nonlinearity (DNL) and Integrated nonlinearity (INL)

Table I. Performance comparison

	[6]	[7]	[9]	[10]	This work
Technology (μm)	0.18	0.18	0.18	0.18	0.18
Supply (V)	1	0.6	0.6	0.8	0.9
Resolution (bit)	10	10	10	10	12
Sampling rate (kS/s)	100	100	20	200	200
ENOB (bit)	9.4	9.3	9.4	9.05	9.9
Power consumption (μW)	3.8	1.3	0.038	0.2	2.72
FoM (fJ/conv·step)	56	21	2.8	1.88	28
Area (mm^2)	0.240	0.125	0.163	0.105	0.127

6 Conclusion

This paper presents a low power SAR ADC with a novel ladder-based time-domain comparator. The delay, gain and noise performance of the proposed comparator is analyzed. By using a novel LB VCDL, a better noise performance is achieved

compared to existing arts. The proposed ADC is fabricated in a standard 0.18 μm CMOS process. With a power supply of 0.9 V, the total power consumption is 2.72 μW at the sampling rate of 200 kS/s. The measured ENOB is 9.9 bits and the corresponding FOM is 28 fJ/conv·step.

Acknowledgements

This work is sponsored by National Natural Science Foundation of China (No. 61371032) and the Fundamental Research Funds for the Central Universities. It also gains support from the Analog Devices, Inc. (ADI). The authors would like to thank Mr. Monton Zhao, the senior engineer of ADI and his colleagues, for their useful discussions and instruction.