11b 60 MHz pipelined ADC with inverter-based class AB amplifier in 28 nm CMOS technology

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Abstract: An inverter-based class AB amplifier is proposed to design the 11b pipelined analogue-to-digital converter (ADC) in 28 nm CMOS technology. The structure of the proposed amplifier is more concise compared with conventional amplifiers. The amplifier occupies small area, and its quiescent dissipation is only 1.4 mW. This structure is suitable for design in scaled process. The operation of the amplifier is carefully elaborated. The simulation results show: the ADC can achieve 75.3 dB SFDR and 66.8 dB SNDR, while it occupies an area of 0.4 mm² and consumes a power of 17 mW with 1.05 V supply. These results yield a FOMS of 159.3 dB.

Keywords: ADC, inverter-based, amplifier, small area

Classification: Integrated circuits

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1 Introduction

The power efficiency of high speed, high precision pipelined ADC is mainly decided by the amplifier used in switched-capacitor circuits [1, 2]. It meets more difficulties to design traditional operational amplifiers (OPAMPs) in modern, scaled CMOS process, because of the low supply voltage and low intrinsic transistor gain. The low supply voltage means small output swing, and the low intrinsic transistor gain means low-accuracy amplification. Some effective techniques, such as folded-cascode, gain boosting, multi-stage amplification and digital correction, have emerged to realize high-performance OPAMPs. However, it often increases the power consumption and design complexity of the OPAMPs using these techniques. Some inverter-related techniques [1, 3, 4] have been used in the amplifier to improve the efficiency. However, the technique in [1] uses passive devices; [3] would get low bandwidth using the technique; and the technique in [4] uses extra switch and bias voltage. So, in this work, an inverter-based class AB amplifier is proposed to design the 11-bit pipelined ADC based on 28 nm CMOS technology. The inverter-based input stage can double the gain compared with the conventional one. Also, a kind of class AB circuit is adopted to realize rail-to-rail output with small current [5]. In this work, the structure of the proposed amplifier is described, and its benefits are analyzed. In order to have a deeper understanding of the amplifier’s operation, the Multiplying Digital-to-Analog Converter (MDAC) is elaborated as an example of switched-capacitor circuits. The switched-capacitor comparator circuit is also described in this work.

2 Circuits design

2.1 Inverter-based class AB amplifier

The proposed amplifier utilizes a fully differential structure, which uses MOSTs in the linear region for the common-mode feedback (CMFB). The amplifier is depicted in Fig. 1, and it is comprised of three stages. The input stage is an inverter, and the two stages back realize low-voltage class AB output. The main advantage of this output scheme is that nodes 2 and 2' can have very large swings. The output stage can sink and source currents which are much larger than the quiescent currents. Stability problems have to be carefully resolved because the amplifier has three poles at nodes 1, 2(2'), and 3. Pole splitting technique can be applied to ensure the stability of the amplifier. The dominant pole is at node 3, because the capacitor at node 3 is much larger than the capacitor at node 1 and 2. So, the output resistor should be increased to reduce the dominant pole. Thus, the output transistors can be set to work in the sub-threshold region. Another important issue is the gain of the amplifier. In fact, a gain of 72 dB is easily obtained from an

amplifier of three stages to meet the precision demand of the 11b pipelined ADC. As the output transistors of the proposed amplifier work in sub-threshold region, their gain would be enhanced by the output resistors' boosting compared with transistors in normal region (such as saturation region). Then, the proposed amplifier can have more than 80 dB gain, which will generate enough margin to guarantee the ADC's accuracy.

Fig. 1. Proposed inverter-based class AB amplifier

Fig. 2. Frequency response of the amplifier

Frequency response is simulated using a load capacitor of 2 pF. Fig. 2 shows the magnitude and phase response of the amplifier, it can be seen that the DC gain is 80.1 dB, the GBW (gain-bandwidth product) is 736.8 MHz, and the PM (phase margin) is 60.15 degree. Also, PVT (process, voltage and temperature) analyses are carried out to show the robustness of the proposed amplifier. The process corners used are tt, ss, ff, fnsp and snfp, with a temperature variation from -40 to 80°C and using a nominal VDD of 1.05 V with $\pm 10\%$ variations. Table I summarises the frequency response specification with the minimum and maximum values. Monte Carlo (1000 samples) simulations are carried out to show the impact of the mismatch in Fig. 3. The results of the PVT and Monte Carlo analyses show that the proposed amplifier could satisfy the ADC's application requirements.

Table I. Results of the PVT analyses

specification	Typical	minimum	maximum
Gain/dB	80.1	77.8	85.2
GBW/MHz	736.8	602.3	892
PM/degree	60.15	51	72.5

Fig. 3. Results of the Monte Carlo simulation

2.2 Analysis of the amplifier's operation

The 1 stage CMFB in the proposed amplifier may be not enough to make the common mode output voltage stable, since the amplifier has 3 stages. Also, the common mode output voltage could not be well defined using the linear region MOSTs for the CMFB. So, the MDAC structure of [6] showed in Fig. 4 is used to enhance the common mode feedback. This structure could realize the normal amplification function because the differential-mode gain is two, while it can also make the common output voltage stable due to the common mode gain is one. The transient waveforms of the MDAC are showed in Fig. 6. As can be seen in Fig. 6, the common output voltages $(V_{OP} + V_{ON})/2$ are similar to the common input voltages $(V_{IP} + V_{IN})/2$, and they are both around $1.18 \text{ V}/2 = 0.59 \text{ V}$, which shows the common mode gain is one. The differential output voltages is $V_{OP} - V_{ON}$, and the differential input voltages is $V_{IP} - V_{IN}$. The reference voltage V_{ref} is set to be 0.5 V . As can be seen in the zoomed region: $V_{OP} - V_{ON} \approx 2(V_{IP} - V_{IN}) - V_{ref}$, where $V_{OP} - V_{ON}$ is 498.5808 mV and $V_{IP} - V_{IN}$ is 499.3539 mV , which shows the differential-mode gain is two.

When the MDAC works in amplification phase, the proposed amplifier would start to charge the capacitors as Fig. 5: first, operating like digital circuits; then, operating in steady state. A key issue is the design of output transistors, because it affects the charging speed and the stability (the load to the second stage and the dominant pole) of the amplifier. The charging is slew-based, and the charging speed is mainly decided by the maximum current. The output transistor operates in saturation region in charging state, and operates in sub-threshold region in steady state. So, the following relations could be obtained,

$$\text{charging speed} \propto \frac{W}{L} * V_{GS, \max} \quad \text{stability} \propto \frac{L}{W} * \frac{1}{\exp(V_{GS, \text{steady}})}$$

Where W is the width, L is the length, V_{GS} is the gate-source voltage of the output transistor. According to the above relations, it can be concluded that the charging speed and the stability change toward different trends when the parameters of the

output transistor changes. So, the charging speed and the stability should be considered simultaneously when designing the output stage of the amplifier. And the DC, AC and TRANSIENT simulations should be all carried out carefully to design the amplifier.

Fig. 4. MDAC used in ADC

Fig. 5. Operation of proposed amplifier

Fig. 6. Transient waveforms of MDAC

2.3 Operation of comparator including switches and capacitors

The switched-capacitor comparator circuit is described in Fig. 7. Non-overlapping two-phase clocks clk1, clk2 are used in the circuit. The simulation results is showed in Fig. 8. As can be seen from Fig. 8, when clk1 is high, the input signal is sampled; and the voltages of the comparator's input nodes A,B are set to be Vcm. When clk2 is high, the voltages of nodes A,B change for comparing, then the comparator will make a comparison and generate digital output code Q.

Fig. 7. switched-capacitor comparator circuit

Fig. 8. Transient waveforms of comparator circuit

3 Simulations and comparisons

The proposed ADC is designed base on 28 nm CMOS technology. The ADC's layout is showed in Fig. 9, which consists of a sample-hold stage and nine identical 1.5-bit MDAC stages followed by a 2-bit backend flash ADC. Reference buffers are also placed in the chip to provide internal reference voltages. The proposed amplifier's area is only 28 μm * 26 μm due to its inverter-based structure, and it consumes a quiescent power of 1.4 mA. The ADC core occupies an area of 0.4 mm * 1 mm. At 60 MHz sampling rate, the ADC achieves 75.3 dB SFDR and 66.8 dB SNDR for a Nyquist frequency input. The simulation results of dynamic performance are plotted in Fig. 10. The total power consumption is 25 mW, and the power consumption excluding reference buffers is 17 mW. The FOMS [7],

$$\text{FOMS} = \text{DR}_{\text{dB}} + 10 \log \frac{\text{BW}}{\text{P}}$$

a more accurate measure for noise-limited ADCs, is 159.3 dB.

Fig. 9. Layout of proposed 11b pipelined ADC

Table II summarizes and compares the performance of the proposed ADC with other works. To provide a fairer comparison, the resolutions are all above 11 bit, the sampling rates are all above 50 MHz, and the power consumption of on-chip reference buffers has been excluded from all the ADCs.

Fig. 10. FFT spectrum of proposed 11b pipelined ADC.

Table II. Performance comparison of pipelined ADCs

	[7]	[8]	[9]	[10]	This work
Technology (nm)	40	90	180	40	28
Power supply (V)	1	1.2	1.6	1.8	1.05
Resolution (bits)	12	12	14	11	11
Fsampling (MHz)	195	200	60	300	60
SNDR at Nyq. (dB)	64.8	59.4	73.3	56.6	66.8
SFDR at Nyq. (dB)	82	/	84	/	75.3
Area (mm ²)	0.81	1.36	1.43	0.42	0.4
Power (mW)	53	186	67.8	40	17
FOMS (dB)	157.5	146.7	159.8	152.4	159.3

4 Conclusion

In this letter, an inverter-based class AB amplifier is used to design the 11b 60 MHz pipelined ADC. The proposed amplifier occupies small area, consumes little power, and is easy to design compared with the traditional amplifiers. The simulation results and the comparisons show that the ADC of this work can achieve a good FOM.

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