Ultra low power and highly linearized LNA for V-band RF applications in 180 nm CMOS technology

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Abstract: In this study, the common gate stage of the conventional inductive degeneration cascode LNA operating in 60 GHz V-band for the upcoming Wi-Fi standard, and 802.11ad standard with data rates up to 7 Gbit/sec was linearized by bilateral CMOS resistor. The proposed method linearizes the LNA by 6 dBm with minimum power consumption. The proposed LNA dissipates only 2.05 mW supplied from 1.8 V voltage source and exhibits a minimum noise figure of 6.8 dB in the operating frequency. The LNA, without the proposed linearization technique, exhibited 7 dB gain. The linearized LNA exhibited 3.5 dB gain. The ADS2016.01 with TSMC 180 nm CMOS model files were used to perform the simulation.

Keywords: linearity enhancement, CMOS LNA, 180 nm process

Classification: Microwave and millimeter-wave devices, circuits, and modules

References


1 Introduction

The plethora of the new applications that need to utilize the V-band spectrum allocation for its high-speed data rate, such as, the upcoming 802.11ad, satellite links, point to multipoint communications, and new Wi-Fi services, created the need to study the linearization of the receivers in this band in order to reduce interference power. A prior study showed that the three-cascaded LNA designed in the 60 GHz front-end receiver consumed 43.2 mW with minimum noise figure of 8.8 dB providing 12 dB peak power gain [1]; however, the high power dissipation and high noise figure were the two major issues for V-band receivers. In another study, the single stage V-band LNA exhibited 9.6 mW power dissipation and 5 dB gain [2]. In a recent study, the LNA in the 802.11ad CMOS receiver exhibited an IIP3 of −7 dBm with high power consumption of 30 mW [3]. Despite of the good power gain and noise figure obtained in the study, the linearity and high power consumption still considered serious issues. Another work showed that the LNA in the 90 nm CMOS 60 GHz receiver exhibited 14.5 mW power consumption with 12 dB power gain [4]. Moreover, the two stage LNAs provided good gain, but the power consumption still needed to minimize. Most recent studies showed high power consumption and did not consider the linearity as an issue despite its other good characteristics, such as, high gain and low noise figure, for example, the gm boosted LNA exhibited an IIP3 of −26 dBm with 8.9 mW power dissipation with 30 dB power gain [5]. The bidirectional 60 GHz low noise amplifier power amplifier exhibited high power dissipation of 39.6 mW, which need to be reduced for the next wireless generation [6]. In addition, the 60 GHz ISM band LNA dissipated 20.4 mW [7]. The variable gain LNA implemented in 65 nm CMOS consumed 28.8 mW with power gain of 19.8 dB [8]. It was verified that as the frequency increased, the linearity of the common gate stage highly affected the cascode LNA IIP3 directly [9]. Furthermore, the linearized 2 GHz CMOS LNA mitigated the nonlinearity effects of the common gate stage through passive resistor at the drain [9], however, in the V-band frequencies, the nonlinear current components increased dramatically and even the tuned passive drain resistor could not mitigate the effects of the nonlinear leakage current of the common gate stage. Therefore, in the current study, we utilized the bilateral CMOS switch to find an optimum load impedance that maximize the IIP3 of the 60 GHz cascode LNA.
2 Design methodology

The proposed LNA is shown in Fig. 1.

![Proposed 60 GHz cascode LNA](image)

The bilateral CMOS switch connected to the drain of the common gate stage leads to an equivalent resistance of $r_{on}$ that can reduce the total drain resistance of the common gate stage of the LNA cascode. The switch voltage and the lengths and widths of transistors of M4 and M5 were optimized to an optimal value that maximized the total IIP3 of the cascode LNA. The ADS optimization tool was used for this purpose and yielded lengths of 0.18 µm and 9.2 µm for M4 and M5, respectively. Moreover, the widths of M4 and M5 were optimized to 0.84 µm and 0.193 µm, respectively. In addition, the switch voltage was optimized to 1.8 V. The total switch impedance reduces the effects of the total output resistance to an optimum value that maximizes the IIP3, however, this tradeoff is useful in receivers that require high linearity LNA to suppress the effects of the interferes. Fig. 2 illustrates how the combined transfer function of the NMOS and PMOS MOSFETs varies with the switch voltage [10].

The Ld and Cd resonates at 60 GHz, the optimum widths of the M1 and M2 transistors were designed to be 6.62 µm. The matching components were designed with smith chart utility tool to match the input and output port to 50 Ω. The coupling capacitors of 1 pF were necessary to prevent any DC variation to the biasing of M1 and M2. The M1 and M2 overdrive voltage were taken 0.3 V and biased by the constant current source in Fig. 3.
The Pn tone test with frequency spacing of 10 MHz results in the two interferes frequencies equal to 59.995 GHz and 60.005 GHz entering to the linearized LNA. The resultant IIP3 of 0 dBm was obtained as shown in Fig. 4.

Where

\[ IIP_3 \text{ (dBm)} = \frac{\Delta P}{2} + P_{in} \]  

The S-parameters indicates forward power gain of 3.543 dB with input and output losses of less than 20 dB as shown in Fig. 5.

The noise figure of the proposed LNA is 6.79 dB as shown in Fig. 6. Meanwhile, the total power dissipation of the circuit is only 2.05 mW including the biasing stage supplied from 1.8 voltage source.
The cascode LNA exhibited gain of 7 dB, noise figure of 6.641 dB, and an IIP3 of −6 dBm. The S-parameters, NF, IIP3 of the current reuse designed circuit are shown in Figs. 7, 8, and 9, respectively. The circuit consumes only 2 mW including the biasing stage.
Fig. 7. Cascode LNA S-parameters

Fig. 8. Cascode LNA NF

Fig. 9. Cascode LNA OIP3
4 Conclusion

The effects of the common gate stage on the linearity of the 2 GHz LNA cascode structure was widely investigated by [9]. However, in the 60 GHz cascode LNA, the common gate stage leakage current grows dramatically and hence worsens the IIP3. At V-band frequencies, the optimum resistor connected at the drain of the common gate stage to optimize the load impedance for minimum IIP3 was found to be 8 MΩ. Such impractical value of this resistor increases the noise figure and rises the need to replace it by an alternative circuit whose impedance maximizes the IIP3 sacrificing the LNA gain. A tradeoff between those two criteria can lead to optimum LNA performance. The proposed method in the current study enhances the linearity with 6 dBm variation at the cost of 3.5 dB reduction in gain due to the mandatory tradeoff between the gain and linearity. However, a reduced power consumption of 2 mW, including the biasing stages, could be achieved in the proposed LNA, which leads to minimizing the entire RF-frontend receiver power consumption.

Table I. Proposed LNA specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency/GHz</td>
<td>60</td>
</tr>
<tr>
<td>Gain/dB</td>
<td>7/3.5*</td>
</tr>
<tr>
<td>IIP3/dBm</td>
<td>−6/0*</td>
</tr>
<tr>
<td>Power consumption/mW</td>
<td>2.05</td>
</tr>
<tr>
<td>NF/dB</td>
<td>6.64/6.793*</td>
</tr>
<tr>
<td>S11/dB</td>
<td>&lt;−20</td>
</tr>
<tr>
<td>S22/dB</td>
<td>&lt;−20</td>
</tr>
</tbody>
</table>

*Means the specification after linearization