A 400-MS/s 10-b 8 interleaved SAR ADC in 0.13 um CMOS

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Abstract: This paper presents an 8-channel time-interleaved SAR ADC. A novel sampling structure is proposed to improve the input bandwidth which also avoids time-skew calibration. The comparator offset cancellation is achieved by body voltage adjustment using low-power charge pump. Each channel has its own on-chip reference buffer to stable reference voltage and correct gain mismatches. The prototype is fabricated in 1P6M 0.13 µm CMOS technology. At 400 MS/s, the ADC achieves an SNDR of 50.84 dB and 45.7 dB at 19.1 MHz and 451 MHz, respectively. It consumes 200 mW, resulting in FOM of 1.76 pJ/con-step.

Keywords: analog-to-digital converter, SAR, time-interleaved, offset calibration, adjustable reference buffer

Classification: Integrated circuits

References

1 Introduction

Recently, time-interleaved (TI) ADCs have become critical components in high-speed wireline and wireless communication systems. They directly increase the conversion rate of a data converter by using a number of converters working in parallel for a simultaneous quantization of input samples. In addition to improving the sampling rate, they can also reduce the die size and relax the requirements on fabrication process at the same time [1, 2].

Nowadays, SAR ADCs are attractive to design high-speed and medium resolution converters with low power and small area. Besides, one unique character of SAR ADC slice is that the main clock is non-50%-duty. When SAR ADCs were interleaved and proper number was selected, only one sample-capacitor is connected to the input at a time, lowering the input capacitance. Thus, SAR ADCs are good choice to design high speed and power-efficient TI ADCs [3, 4].

This paper presents a TI SAR ADC with 8 channels. For high-speed sampling, a sampling capacitor is used apart from the capacitor DAC. The master-clock-control sample-switch technique is adopted to suppress the time-skew effect among channels. Besides, body-voltage trimming method is used to calibrate the offsets of the comparators. Each sub-ADC receives its own buffered reference voltage, which is digitally set by a current DAC to calibrate the gain mismatches between slices.

2 Proposed ADC architecture

The architecture and timing diagram of the proposed ADC operating at 400-MS/s sampling rate is illustrated in Fig. 1 which consists of 8 interleaved 10-b 50-MS/s SAR ADCs followed by a combining multiplexer that combines the 8-channel datas into ones. For simplicity, the architecture is described with a single-end version. A maximum 1.2 $V_{pp}$ differential input signal with 0.6 V common mode is delivered to the sub-ADCs via an on-chip source follower buffer in order to limit kickback noise back to the input end. A 500 IF small capacitor is used instead of
the capacitor DAC (CDAC) as the sampling capacitor to get high input signal bandwidth and reduce the loading of input buffer. Additionally, the bottom-plate sampling is utilized to ensure the linearity of the sampling [5]. The sampling instances of TI channels are synchronized with the same master clock $C_{8}$, which is selectively applied to each channel via an MUX controlled by the clock signals $C_{en1}$ to $C_{en8}$. By minimizing the number of transistors between the master clock and the sample switch, time skews between channels are minimized as well [6, 7]. After sampling, each SAR sub-ADC resolves 10b of binary-scaled compensation weight with two extra redundant bit-cycles in 12 clock cycles to alleviate the DAC settling problem and speed up the conversion [8]. The splitting-monotonic with the monotonic capacitor switching procedure is utilized to simplify SAR logic and achieve less common mode variation [9]. The bottom-plates of the capacitor arrays are either connected to $V_{refp}$ or $V_{refn}$. The sequence of conversion steps is managed by the SAR logic that generates the asynchronous control signals for the com-

Fig. 1. The proposed time-interleaved SAR ADC.
parator and switches. The direct switching technique is employed which the corresponding switching capacitor is pointed before the comparison decision. Once the comparator makes a decision, the output directly transmits to the capacitor switching buffer and switches the right reference voltage to the corresponding capacitor [9]. A double tail dynamic comparator with background offset calibration is adopted. At the end of the SAR conversion, the CDAC and sampling capacitor are reset with the signal $\phi_{reset}$. Comparator calibration is initiated at the same time and prior to the next sampling phase $\phi_{ini}$. Each channel has its own reference buffer which achieves better isolation. The reference voltage can also be adjusted easily to correct gain mismatches based on external algorithm.

3 Circuit implementation

3.1 Low timing skew interleaved sampling

Calibration of timing mismatch requires high-frequency test signals and complicated calibration algorithms. For TI ADCs, the timing skew per channel can be approximated by a Gaussian distribution. The SNR caused by timing skew is [6]:

$$SNR_{\sigma_t} = 1/(\sigma_t \cdot 2\pi \cdot f_{in})$$

(1)

with $\sigma_t$ is the RMS value of the timing skew. For an SNR of 50 dB and input frequency of 500 MHz, the required timing skew between channels should be smaller than 1 ps RMS. In this design, a good timing alignment is achieved by using a master clock to synchronize the different sampling instants. The sampling instant of each channel is defined by the opening of the bottom-plate switch. In order to reduce the timing errors, the number of components in the path from the common master clock to the sample switch should be minimized. As shown in Fig. 2(a), the components between the sampling signals ($\phi_s$) and the common master clock signal ($\phi_m$) are only a pass-gate. When the $\phi_{esti}$ is high, the master clock switch enable the discharge paths of the bootstrapped switch through the pass-gate. The main switch was turned off once its $V_g$ was below ($V_{th} + V_{cm}$). The $\phi_{esti}$ works once the conversion is over and prepares for offset calibration and next sampling. An improved bootstrapped switch [2] is used to pass the constant voltage, $V_{cm}$, for low on-resistance shown in Fig. 2(b). Thanks to the simplified structure, a small hold MOS capacitor can be adopted. As node A exceeds the $V_{DD}$, the node C drops and MP2 turns on in a very short time. Compared to conventional method, a smaller switch can be used which improves the falling slope of the switch.
and the whole timing character. In summary, only five transistors (MN1, NM2, NM3, MP1 and main switch) cause timing skews. Besides, matched lines in the layout are used (same width, length and spacings) to distribute clock and input signals to the channels [10]. The post-simulated variation of time skew from 500 Monte Carlo is 500 fs. Such a solution can result in an ENOB greater than 8 bit at 500 MHz in over 95% of samples.

3.2 Dynamic comparator with background offset calibration

Comparator is a key component of the conversion in SAR ADC. Fig. 3(a) depicts the proposed dynamic comparator, modified from the one in [11]. The double-tail latch type comparator allows its speed and offset to be optimized independently. In TI SAR ADC, mismatched offsets in various channels lead to a repetitive pattern with period \(N/fs\) that causes tones at \(fs/N\) and its multiples. The SFDR is turned to:

\[
SFDR \approx 20 \cdot \log \frac{\pi V_{FS}}{8V_{ox}}
\]  

(2)

The offset mismatches must be small than 0.195 LSB to achieve 62 dB SFDR with a 99% yield [12]. In this paper an offset cancellation technique based on body voltage trimming is presented in Fig. 3(b). By modifying the body voltages of the input transistors, the threshold voltage can be changed which can be expressed as follows:

\[
|V_{th,p}| = |V_{th0,p}| + |\gamma|(\sqrt{2\phi_f} + |V_{SB}| - \sqrt{2\phi_f})
\]  

(3)

where \(|V_{th0,p}|\) is the threshold voltage at \(|V_{SB}| = 0\), \(\phi_f\) is the Fermi voltage and \(\gamma\) is the body-effect coefficient. The relationships between leakage current, \(V_{th}\) and

![Fig. 3. (a) The proposed dynamic comparator. (b) The offset cancellation technique.](image-url)
the body voltage of PMOS are shown in Fig. 4(a). To ensure the reverse-biasing condition of the source-body junction, the body of one of the inputs is fixed to 1 V while the body of the other is changed within the allowed possible range (from 800 mV to 1.2 V). It can be seen that the $V_{th}$ can vary about 52 mV ($\pm 26$ mV) by changing the body voltage ($\pm 200$ mV) to compensate the effect of offset mismatches. This technique does not introduce any additional capacitive loading in the analog path [13]. For low-power consumption and fine offset calibration, a charge-pump-based offset tracking method was used. Depending on the decision of the comparator, charge is either added to the calibration capacitor $C_{cal}$ or subtracted from it. The offset calibration is operated in every last cycle of conventions. The $C_p$ is the parasitic capacitors of the switches and routing and about 1 fF according to postlayout extraction. In order to reach the resolution of $0.195$ LSB ($228\, \mu$V), the size of the $C_p$ is at least 580 fF. Additional, the vibration from the comparator will feed through to the $C_p$ that affects the accuracy of calibration. Inserting a resistor and a bigger $C_p$ can relief the feedthrough effects. So, the The ratio of the hold capacitor $C_p$ and the update capacitor $C_{cal}$ are chosen to be $C_p : C_{cal} = 1 : 1500$ for needed offset accuracy. The non-overlap signals to avoid simultaneous conducting of two PMOSs or NMOSs which will affect the accuracy of calibration. The 50 post-simulation results before and after calibration are illustrated in Fig. 4(b). The 1-sigma offset value before calibration is 5.5 mV, while it has been remarkably reduced to 65 $\mu$V after calibration which meets design requirements. The total calibration circuits only cost 50 $\mu$W.

![Graph](image)

**Fig. 4.** (a) Leakage current and $V_{th}$ vs the body voltage of PMOS (b) Monte-Carlo simulations of comparator offset

### 3.3 On-chip adjustable reference voltage buffer

For a high-speed SAR ADC, the CDAC network must settle in a few hundred picoseconds, which requires a high-speed reference buffer to provide fast charge recovery capability. Thanks to the redundant algorithm, the supply variation can be tolerated for the MSB cycles, which relaxes the bandwidth requirement of the reference buffer. The replica-driving reference buffer has been adopted as shown in Fig. 5 [14]. The feedback loop assures stability with low power consumption while the open-loop settling due to the replica stage enables fast operation. Native NMOS and forward-bias-body PMOS were used to relief the headroom of low supply voltage and share the one current branch for low power design. The transistors in
two SFs were designed with proper size and careful layout to reduce the mismatches between them. The current densities for the two branches are designed to be the same \((W/L)_1 = (W/L)_2 = \frac{1}{m}\) such that their outputs match. During capacitor switching in the DAC, the voltage change on \(V_{\text{refp}}\) and \(V_{\text{refn}}\) will couple through \(C_{\text{gs}}\) of M1 and M2 which perturbs the feedback loop. \(R_0\) and \(C_0\) act as a low pass filter to isolate the disturbance from the ADC. Resistor \(R_1\) were inserted in the feedback loop to adjust the reference voltages by an 8 bit current-DAC. The adjustment range depends on the product of differential current of the DAC and resistance of \(R_1\). The gain of each channel can be changed with 256 steps (0.05% per step) which satisfy 10 bit resolution.

\[
(W/L)_{1(2)} : (W/L)_{1R(2R)} = 1 : m
\]

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![Fig. 5. The adjustable replica-driving reference buffer.](image)

4 Measured results

The prototype ADC was fabricated in SMIC 1P6M 0.13 \(\mu\)m CMOS process and mounted in a plastic QFN88 package. The die micrograph is shown in Fig. 6(a). The total chip area is \(2 \times 3 \text{ mm}^2\), the measured output spectrum is shown in Fig. 6(b) when a 19.1 MHz input sine wave is sampled at 400 MS/s. Its signal-to-noise-and distortion ratio (SNDR) is 50.84 dB and spurious-free-dynamic-range (SFDR) is 61.24 dB. The static performance of differential non-linearity (DNL) and integral non-linearity (INL) is shown in Fig. 7(a). The measured DNL and INL are +0.46/−0.45 LSB and +0.50/−0.33 LSB, respectively. Fig. 7(b) plots the SNDR and SFDR of the ADC as a function of the input frequency. The ADC maintains linearity over 7.3 bit until the input frequency is beyond 451 MHz. The total power consumption of the prototype ADC is 200 mW (including input buffer, SAR ADCs, reference buffers, and clock generation) and a figure-of-merit (FOM) at 1.76 pJ/covn-step is achieved.
5 Conclusion

This paper presents a 8-channel interleaved SAR ADC fabricated in 0.13 µm CMOS technology. A novel sampling structure is implemented to improve the bandwidth and avoid time-skew calibration. A background offset calibration and on-chip adjustable reference buffer are used to calibrate offset and gain mismatches between channels. The proposed ADC achieves an ENOB over 7.3 bit up to 450 MHz input frequency at 400 MS/s.

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