Cost-effective 97%-efficiency charge-pump voltage balancer for multi-level PWM photovoltaic micro-inverter

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Abstract: In this paper, cost-effective high-efficiency photovoltaic (PV) power conditioning system (PCS) applicable for small-scale grid tied micro inverters usually under 400 W is proposed. The two-stage PCS consists of a modified H-bridge topology producing 5-level output and a boost converter magnetically-coupled with a secondary charge-pump circuit to provide charge balancing with isolation. Compared to the previous multi-level micro-inverter systems, the inverter circuit has reduced the part count, the DC-DC stage enables Maximum Power Point Tracking (MPPT) without power-conversion efficiency compromise during the voltage balancing operation at the neutral point of the DC-link capacitor for a low-cost 5-level photovoltaic inverter. Also, the voltage ratios are automatically maintained by the coupled-inductor turns ratio, thereby eliminating the additional control circuit for maintaining voltage balancing. Proposed micro-inverter topology is proved by the simulation and hardware prototype experiments.

Keywords: charge-pump, coupled-inductor, low cost, voltage balancer

Classification: Power devices and circuits

References


1 Introduction

There is significant increase of interest in micro-inverters designed for photovoltaic (PV) systems, due to the growth in market for PV residential applications [1, 2, 3]. Several multi-level inverter topologies designed for PV systems with reduction in leakage current and increase in number of the output-voltage levels have been proposed [4, 5, 6, 7]. A modified H-bridge inverter in Fig. 1 produces 5-level output voltage with minimum increase of parts count, thereby providing optimum efficiency, reliability and reduction in leakage current. In the previous multi-level inverter, however, the voltage balancing operation at the neutral point of the DC-links between $C_{dc1}$ and $C_{dc2}$ was not realized, since the pre-regulator operates for PV power conditioning, not for the balancing [8, 9]. Recently, a solution using a multi-output flyback converter for both of the voltage balancing and the power-conditioning MPPT operation is proposed in [10]. The circuit is shown in Fig. 1(a).

Since the secondary two coils have the same winding number, the outputs $(V_{dc1}, V_{dc2})$ automatically have the same voltage. However, one of the major drawbacks of this topology is that the efficiency of the multi-output flyback converter is relatively low. This drawback from the previous iterations is improved in the proposed topology in a cost-effective and efficient manner. In this paper, a new two-stage micro-inverter is proposed using the modified H-bridge topology and a boost converter coupled with charge-pump circuit. The proposed micro-inverter topology is cost-effective and power-efficient due to its reduced part count and without power efficiency compromise during the voltage balancing at the neutral point of the DC-link capacitor. The circuit diagram for the proposed micro-inverter topology is shown in Fig. 1(b).

The DC-AC stage consists of a modified H-bridge inverter with 5-level output. It has reduced number of parts count compared to previous 5-level inverter topologies [10]. A Sinusoidal Pulse-Width Modulation (SPWM) operating a one leg of the H-bridge at fundamental frequency (50/60 Hz) is used to optimize the
efficiency of the micro-inverter. A drawback exists in the inverter that the lower-level input diode \((D_h)\) draws greater current from the low cap \((C_{dc2})\) than the upper switch \((S_h)\) does. So, the inverter requires an extra voltage-balancing circuit for the DC-link capacitors. The DC-DC stage of the proposed micro-inverter consists in two parts: a boost converter and a coupled-inductor charge-pump circuit. The boost converter provides the power for the lower DC-link \((V_{dc2})\) and the charge-pump circuit provides power to the upper DC-link \((V_{dc1})\). The key feature is that the voltage ratio between the boost output and the charge-pump output is fixed regardless of the switch turn-on time or of the load current. Hence, the voltage balance is automatically maintained even under light-load conditions without addition of extra power/controller circuits.

2 Operating principle for the proposed micro-inverter

The current flow of the DC-DC stage during turn-on/off of switch \(S_b\) is shown in Fig. 2. As the figure, during turn-on, the inductor and the charge-pump capacitor are charged simultaneously. During turn-off, the energy stored in the boost inductor is transferred to \(C_{dc2}\), while the charge-pump capacitor discharges to \(C_{dc1}\). The voltage gain for the boost and charge-pump output is respectively derived as,

\[
\frac{V_{dc1}}{V_{pv}} = \frac{1}{1 - D} \frac{N_s}{N_p}, \quad \frac{V_{dc2}}{V_{pv}} = \frac{1}{1 - D}.
\]

So, if we set \(N_s = N_p\), then the voltages become identical. Fig. 3 shows the reference signals for each switch used in PWM strategy. Since the switching signal for switch \(S_3\) an \(S_4\) are complementary, the right-leg of the modified H-bridge operates under fundamental switching frequency. The switch \(S_0\) operates only during the higher voltage levels in positive and negative half-cycles.
3 Control scheme and loss calculation

3.1 Control scheme

The control scheme for the proposed topology under grid-connected operation is shown in Fig. 4. The controller for the 5-level inverter consists of a cascaded type two-loop controller. The inner loop consists a high bandwidth current loop to inject low THD current under unity power factor to grid, while the outer loop voltage controls the lower DC-link voltage ($V_{dc2}$). Since the transformer turn ratio is fixed as 1:1, the upper $V_{dc1}$ is automatically maintained the same. The transfer functions required for the design of the two-loop controller are derived in (2),

$$\frac{V_{DC2}}{d1} = \frac{V_{DC2}}{2sL}$$

$$\frac{V_{DC}}{Vc} = \frac{MV_o}{k} \left[ \frac{1}{2 + sCr_i} \right]$$

where $M$ is the modulation index, $k$ is the scaling factor and $r_i$ is the input small-signal resistance, $d_1$ is inverter duty cycle, $V_c$ is the inverter control voltage.

A rudimentary Perturb-and-Observe (P&O) algorithm is used to track the MPP reference voltage. The transfer function for boost-switch duty ratio $d$ to the PV-voltage in the proposed topology is derived as,

$$G_{pvdl} = \frac{r_{pv}}{d} = \frac{-V_{dc2}}{s^2 L_m C + \frac{sL_m}{r_i} + 1}$$

3.2 Loss calculation and comparison

The power loss for the DC-DC stage in the proposed PCS is derived and compared with the previous multi-output flyback converter in this section.

3.2.1 Conventional multi-output flyback (Fig. 1(a))

EI 60 core was used for the hardware implementation of the 300 W flyback converter. The core loss for the EI 60 core from the data sheet was approximated.
to 2.75 W per 100 W operation. The turns-ratio of the transformer is (1:0.5:0.5). The loss due to leakage inductance (P_leak) is calculated as,

\[
P_{\text{leak}} = 2 \cdot 0.5 \cdot i_{\text{mpeak}}^2 \cdot L_{\text{leak}} \cdot f_{\text{sw}} = 1.9 \text{ W}.
\]

Copper loss in primary (P_{cu-pri}) and secondary winding (P_{cu-sec}) as,

\[
P_{\text{cu-pri}} = i_{\text{mrms}}^2 \cdot R_{\text{pri}} = 1.183 \text{ W}, \quad P_{\text{cu-sec}} = 2 \cdot i_{\text{secrms}}^2 \cdot R_{\text{sec}} = 0.38 \text{ W}.
\]

MBRF40250 in the converter outputs, (V_f) drop power loss = 2V_f \cdot I_o = 1.032 W.

3.2.2 Proposed boost-charge-pump (Fig. 1(b))

MOSFET (IRPF4768) was used in the proposed converter under 50 kHz switching.

Conduction loss: \( (i_{\text{lim}} + i_{\text{ch}})^2 \cdot R_{\text{DS-on}} = 0.041 \text{ W} \).

Switching loss: \( \frac{V_{\text{dsmax}}}{2} f_{\text{sw}} + \frac{1}{2} C_{\text{oss}} V_{\text{dsmax}}^2 f_{\text{sw}} = 0.95 \text{ W} \).

Diode (MBR10200CT) loss due to forward voltage (V_f) drop = V_f \cdot I_o = 0.7 W.

MBRF40250 was used in the charge-pump, the loss = 2V_f \cdot I_o = 0.645 W.

Core loss of the inductor is 0.75 W for 50 kHz operation from the datasheet.

DC loss of the inductor wire is \( P_{\text{wireloss}} = (i_{\text{lim}} + i_{\text{ch}})^2 \cdot R_{\text{DC}} = 0.25 \text{ W} \).

Total loss in the boost-charge-pump converter = 3.34 W \approx (96.6\% \text{ efficiency}).

4 Hardware implementation

The specifications for the hardware prototype are as follows. Maximum power point voltage of the solar array (V_{pv(mpp)}) is 60 V, the solar array current (I_{sat(mpp)}) is 4 A, DC-link voltage (V_{dc1}, V_{dc2}) is 80 V, magnetizing inductance (L_m) is 300 uH, the turns ratio is 1:1. Fig. 5(a) shows the hardware result for the MPPT operation, the MPP voltage is tracked well using the P&O algorithm with DC-link voltage balancing maintained for the constant lower and upper DC-link voltages. Fig. 5(b) shows the 5-level inverter output with the 110 Vrms grid voltage with the DC-link voltages balanced well at 80 V. The THD of the current injected to the grid is calculated as 5.1\% under harsh grid voltage (THD = 3.6\%) conditions.
Fig. 6 shows the comparison between the efficiency plot between the proposed boost-charge pump DC-DC stage versus the previous multi-output flyback converter. The efficiency shows an average increase of 6% throughout the entire output power range. The enhanced efficiency and the cost effectiveness of the proposed topology is shown by the relatively low heat dissipation, resulting in minimal requirement of heat sinks. Fig. 7(a) shows the heat dissipation under 50 W operation while 7(b) shows the result under 300 W operation. It can be seen that maximum heat is dissipated by the boost converter switch $S_b$ (42.1 degrees) and the charge-pump components remain closed to the room temperature, thereby mitigating the application of heat sinks.

![Efficiency Plot](image)

**Fig. 6.** Comparison of efficiency between the proposed boost charge-pump vs. the conventional multi-output flyback converter

![Thermal Images](image)

**Fig. 7.** Thermal image shows heat dissipation of the boost charge-pump stage under (a) 50 W operation (b) 300 W operation. $S_1$ (boost switch) is the hottest spot.

### 5 Conclusion

In this paper, a cost effective 5-level micro-inverter system with charge balancing for PV applications is proposed. The proposed topology enables to perform MPPT operation with a charge balancing operation using the boost converter and the magnetic-coupled charge-pump circuit. This topology is more efficient and cost effective compared to the previous ones in literature. The modified H-bridge topology uses less number of components and enables transformer-less operation for the PV system. The 5-level output voltage helps to enhance the THD of the output, reduces the EMI and enables reduction in output filter size. The proposed topology with its control scheme was validated using a 300 W hardware prototype.

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