A low power consumption inverter-based $\Sigma\Delta$ interface for capacitive accelerometer

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Abstract: A low power dissipation sigma-delta ($\Sigma\Delta$) interface for closed-loop capacitive accelerometer is presented. In order to reduce the power consumption, the front-end circuit blocks work on a much lower frequency than the electronic $\Sigma\Delta$ modulator, and a cascode inverter with dynamic bias is used as an operational amplifier in electronic $\Sigma\Delta$ modulator, reducing the power dissipation greatly and enhancing the immunity to PVT variations. The measured results indicate that, the total power dissipation is 2.2 mW from a 3.3 V power supply. The noise floor of the accelerometer is 7.2 $\mu\text{g}/\text{Hz}^{1/2}$ in a closed-loop operation, and the achieved figure of merit (FOM, 8 pW/Hz) is better than the previously reported works.

Keywords: low power consumption, inverter-based, accelerometer, $\Sigma\Delta$

Classification: Integrated circuits

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1 Introduction

High-precision microelectromechanical systems (MEMS) accelerometers are widely used in inertial and tilting sensing, typically, the design is focus on noise performance, bias stability, dc accuracy. While, according to the market analysis, consumer electronics remain as the leading application field of the MEMS sensors [1]. In this application, except for the criteria mentioned above, the low power dissipation and digital output are very important to be taken into account. Sigma-delta ($\Sigma\Delta$) interface is attractive for MEMS accelerometer since it is simple, provides a digital output, and has a large bandwidth [2]. Many capacitive accelerometer interfaces using direct $\Sigma\Delta$ modulator structure have been published [3, 4, 5], however as the large mechanical and parasitic capacitors must be charged and discharged on the rhythm of the high oversampling clock of the modulator, leading to high power consumption.

In this paper, a low power dissipation $\Sigma\Delta$ interface ASIC for accelerometer is presented, in order to reduce the power dissipation, two methods are applied: the sensors' front-end interface works on a much lower frequency than the electronic modulator, and a cascode inverter with dynamic bias is used as an operational amplifier in electronic $\Sigma\Delta$ modulator, reducing the power dissipation greatly and enhancing the immunity to PVT variations.

2 Implementation of the ASIC

Fig. 1 shows the overall simplified circuit diagram of the closed-loop micro-mechanical accelerometer system. The system consists of micromechanical transducer and a single-end interface circuit. The mechanical transducer consists of a moving proof-mass suspended on springs over a substrate and a set of fixed electrodes. The components of the transducer form a differential pair of capacitors C_{S1} , C_{S2} , whose capacitance are a function of the displacement of the proof-mass.

The readout circuit of the system consists of an exciting signal generator, charge integrator, lead compensator, auto zero and sample/hold, electronic $\Sigma\Delta$ modulator, 1 bit DAC, and clock generator. The sensing element and charge integrator form a capacitance to voltage (C-V) converter, which is shown in Fig. 2(a), transferring a variation of mechanical capacitance to a voltage. In order to compensate the finite gain of operation amplifier, reduce $1/f$ noise and offset, correlated double sampling (CDS) technique is applied in this C-V converter. The lead compensator that is shown in Fig. 2(b) is used to improve the system stability

by positioning a zero closed to the open-loop poles of the mechanical filter. The lead compensator is implemented as a passive filter, which minimizes the power consumption and ensures fast setting. The sample and hold circuit converts a discrete signal to a continuous one, which is dealt with by the following $\Sigma\Delta$ modulator.

In this work, the sensing element just converts a physical signal to an electronic one, rather than is used as a second-order integrator. A third-order cascaded-integrator feed-forward (CIFF) $\Sigma\Delta$ modulator is designed as an electronic filter cascaded with the front-end circuit. A simple RC oscillator is integrated in this chip, no external clock is required to operate this interface circuit. The output of the internal oscillator is a clock with frequency of 512 KHz, which is used for the third-order electronic $\Sigma\Delta$ modulator. The clock of 512 KHz is further divided by a factor of 64 to generate the front-end frequency at 8 KHz.

Compared with previous literatures, there are two differences in this architecture: 1. the third-order $\Sigma\Delta$ modulator works on a much higher frequency, 512 KHz, than the front-end circuit, 8 KHz, to achieve low quantization noise and low power dissipation at the same time. 2. Instead of using of an operational amplifier, an inverter-based SC integrator is adopted to the electronic $\Sigma\Delta$ modulator, which will be discussed in the following section.

Fig. 1. Architecture of the implemented readout circuit

Fig. 2. (a) Schematic of the C-V converter, (b) Circuit diagram of lead compensator

The total power dissipation of the interface can be expressed as:

$$P_{total} = 2f_1 C_{S1} V_R^2 + P_{int} + P_{comp} + P_{SH} + P_{SD} \quad (1)$$

Where the first term denotes the charging and discharging power consumption of the mechanical capacitors, f_1 is the operating frequency, as the mechanical capacitors are far larger than those in other circuits, so the first term is the main

part of the total power dissipation. In addition, P_{int} , P_{comp} and P_{SH} are the power consumption of charge integrator, lead compensator and sample/hold respectively, which are also proportional to the operating frequency f_1 . P_{SD} denotes the power dissipation of the third-order electronic $\Sigma\Delta$ modulator, which is dominated by its operating frequency. In our work, the electronic filter plays the most important role in reducing quantization noise, while, the front-end circuits mainly detect the weak signal, convert it to a continuous voltage and provide it to electronic $\Sigma\Delta$ modulator. Thus, the C-V converter, lead compensator and sample/hold circuit can work on a very low frequency, reducing the power dissipation greatly. While, the electronic $\Sigma\Delta$ modulator operates at a much high frequency to achieve high oversampling ratio and promote SQNR.

A third-order electronic $\Sigma\Delta$ modulator is designed in this work to reduce the quantization noise. Since the electronic $\Sigma\Delta$ modulator operates at a much higher frequency than the front-end circuit, the OPA in the SC integrator will dissipate the most power dissipation. To reduce the power dissipation of OPA, a simple class AB inverter-based SC $\Sigma\Delta$ modulators are proposed in [6], and a gain-boost class-C inverter behaves as a low-voltage subthreshold amplifier for the high-precision requirement is proposed in [7]. However these configurations are very sensitive to PVT variations, the bandwidth, DC point and DC current of inverter all have large fluctuation under different process corners and temperature.

In this paper, a cascode inverter with dynamic bias is proposed, enhancing DC gain and its immunity to PVT variations. The circuit diagram of the inverter-based SC integrator in sampling and integration phase are shown in Fig. 3(a) and (b) respectively. MP1, MP2, MN1 and MN2 compose a cascode inverter, in which the parasitic capacitance between input and output is isolated by cascode transistors. During the sampling phase, MP1 and MN1 are biased by cascode transistors MP3, MN3, and a floating current source composed of MP4, MN4, ensuring that both MP1, MN1 are biased with exactly the same bias currents. During the integration phase, the bias voltages of cascode transistors MP3, MN3 are swapped with those of MP2, MN2, reconfiguring the inverter as a high gain push-pull amplifier with a well-defined bias current, enhancing its immunity to PVT variations.

Fig. 4 shows the schematic diagram of the third-order $\Sigma\Delta$ modulator. It uses a low-distortion configuration, in which the SC integrators do not carry the input

Fig. 3. (a) The inverter-based integrator in the sampling, (b) in integration phase

signal, so that the required linearity of the OPA is reduced, which is quite suitable for inverter operation [8]. The summation of the feedforward path is realized with a parallel connection of capacitors at the comparator input node. As the noise level of the closed-loop system is dominated by the C-V converter, the value of sampling capacitor do not need large.

Fig. 4. Simplified diagram of the third-order CIFF $\Sigma\Delta$ modulator

3 Experimental results

The proposed interface is fabricated in a 0.5 μm CMOS process, occupying an area of $3.2\text{ mm} \times 3\text{ mm}$, as shown in the chip microphotograph in Fig. 5(a). The tested PCB is shown in Fig. 5(b). It dissipates a total current of 0.67 mA from a 3.3 V supply. Most of the current dissipates at the C-V converter, this is because the C-V converter dominates noise floor of the system, a low noise amplifier which needs high static current is essential in it. Additionally, the large mechanical and parasitic capacitor is another important factor. The current of the inverter-based $\Sigma\Delta$ modulator is only 45 μA . In this interface ASIC, the electronic $\Sigma\Delta$ modulator and other SC circuits operate at different frequency, the clock frequency for electronic $\Sigma\Delta$ modulator is 512 KHz, the others operate at the frequency of 8 KHz. The bias for the sensing element is a pulse signal with the amplitude of 3.3 V and the frequency of 8 KHz.

Fig. 5. (a) Photograph of the ASIC, (b) Tested PCB

The 1 bit pulse width modulation (PWM) output is captured by Agilent logic analyzer and post-processed with Matlab. Fig. 6(a) shows the power spectral density (PSD) of the 32768 bitstream, indicating a noise floor of about $-102 \text{ dBV/Hz}^{1/2}$. The sensitivity of the sensor is 1.1 V/g , it achieves a noise floor of about $7.2 \text{ } \mu\text{g/Hz}^{1/2}$, which is mostly dominated by electronic noise. Additionally, the measured spectrum also shows the third-order noise-shaping characteristic as about 60 dB/dec . The result fits the concept of this design, because in this work the noise-shaping function is implemented by the third-order electronic $\Sigma\Delta$ modulator. Fig. 6(b) shows the measured bias stability with 0 g input. A time period of 4 hours'

measured data with sampling interval of 28.8-second is plotted. The figure shows that the maximal output variation within 4 hours is 0.6 mV, and the calculated standard deviation is 0.151 mV, the bias instability of this system is 0.137 mg.

Fig. 6. (a) Output spectrum of the accelerometer (b) Measured bias stability

A summary of the measured specifications of the implemented $\Sigma\Delta$ accelerometer and the comparison with previous works are shown in Table I. A representative figure of merit (FOM) defined as:

$$FOM = \frac{P}{BW * 10^{DR/20}} \quad (2)$$

Where P is the power dissipation, BW is the signal bandwidth, and DR is the dynamic range. In this expression, it takes the power dissipation, noise floor, bandwidth and full scale range into account to evaluate the overall performance of accelerometer. It can be seen that the $\Sigma\Delta$ accelerometer proposed in this work achieves a better performance.

Table I. Performance comparison with previous works

	[1]	[4]	[5]	[9]	[10]	This work
Technology (CMOS)	0.18 μm	0.5 μm	0.6 μm	0.5 μm	0.5 μm	0.5 μm
Supply (V)/Power (mW)	3/3.1	7/23	3.3/12	3/4.5	5/20	3.3/2.2
Bandwidth (Hz)	1000	300	300	500	1500	1000
Noise Floor ($\mu\text{g}/\text{Hz}^{1/2}$)	220	0.2	7.1	4	6	7.2
Full scale (g)/DR (dB)	9.14/92	2/135	11/123	0.1/95	1.5/108	2/109
Sampling rate (kHz)	250	250	1000	40	250	8/512
FOM (pW/Hz)	78	0.03	28	160	53	8

4 Conclusions

A low power inverter-based $\Sigma\Delta$ interface for micromachined accelerometer is presented. In order to reduce power consumption, the electronic $\Sigma\Delta$ modulator and front-end circuit blocks operate at different frequency, and the third-order electric $\Sigma\Delta$ modulator employs inverter as an amplifier. The results indicate that the noise floor of the accelerometer is $7.2 \mu\text{g}/\text{Hz}^{1/2}$, the total power consumption is 2.2 mW.

Acknowledgments

This work is supported by Project of research foundation of the talent of scientific and technical innovation of Harbin (RC2016QN009017).