An effective structure and flow for pre-bond TSV test

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Abstract: Pre-bond TSV test plays a vital role in improving the yield and reducing the cost of 3D ICs. In this paper, we proposed an effective test structure and flow for pre-bond TSV test. In the test structure, the resistor-capacitor parameter related to a specific TSV can be reflected by oscillations with high accuracy. By analyzing the period variations between two oscillations generated in successive test steps, the proposed test scheme enables quick detection of faulty TSVs. Experimental results have demonstrated the effectiveness of the proposed pre-bond TSV test scheme.

Keywords: through silicon via (TSV), pre-bond test, oscillation

Classification: Integrated circuits

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1 Introduction

Through Silicon Via (TSV) provides a promising way to achieve low latency and low power interdie connection and has gained considerable attention in three-dimensional (3D) integration [1, 2]. However, the yield of TSV-based 3D integrated circuits (ICs) is unsatisfactory in the semiconductor industry. One of the major reasons is that various types of defects may occur in the TSV due to the imperfection of TSV manufacturing technology [3]. Typically, several TSV defects can be modeled by two common types of TSV faults, namely resistive open and leakage faults. These TSV faults may induce the performance degradation, or even result in the function failure of 3D ICs. As a result, it is imperative to detect the TSV faults to assure the quality of 3D ICs [4, 5, 6, 7, 8, 9, 10]. The TSV faults are better to be detected prior to the bonding process. By pre-bond TSV test, the die with faulty TSVs can be prevented to be stacked into a 3D IC to avoid unnecessary yield loss.

Design-for-test techniques have been widely researched for pre-bond TSV test [6, 7, 8, 9, 10]. In [6], a pre-bond TSV test technique is proposed based on sense amplification technique and the TSV capacitive characteristics. However, it is relatively difficult to design the analog test structure. In [7], a pre-bond TSV leakage fault test approach is proposed by using the programmable delay line technique. In [8], a non-invasive vernier ring based approach is proposed for pre-bond TSV test. However, the programmable delay line in [7] and vernier delay line in [8] are susceptible to process variations. In [9], ring oscillator (RO) based test structure is proposed for pre-bond TSV test through input sensitivity analysis. By tuning the strength of adjustable driver, two oscillations can be generated to test one TSV. However, this method incurs large test time. In [10], RO based test structure is also applied to measure the oscillation period by taking TSVs as capacitive loads. Two MUXs are inserted for each TSV in the test structure to configure two different ROs [10]. However, the process variations in different components of the two configured oscillators may influence the test accuracy of TSV. Moreover, the MUXs incur more hardware overhead.

In this work, we proposed an effective pre-bond TSV test scheme motivated by the methods in [9, 10], including the test structure and the test flow. The test structure is designed with low overhead and can construct a same oscillation path in different test steps for improving the test accuracy. Moreover, based on the test scheme, on average, the number of oscillations required to test one TSV is approximately only one, thus a smaller test time can be achieved.

2 The proposed pre-bond TSV test structure and flow

In this section, we will firstly describe the TSV model, and then describe the proposed test structure and test flow. Due to the limited space, in this work, we

mainly focus on the detection of resistive-open faults in TSVs. However, similar to [9, 10], the proposed pre-bond TSV test scheme also lays the basis to detect leakage faults in TSVs.

2.1 TSV model

TSV can be modeled by characterizing its R , L , and C parameters. Typically, the R and L of TSV are very small and can be neglected [8, 10]. Hence, as shown in Fig. 1(a), the fault-free TSV can be modeled as a lumped capacitor between TSV and substrate. However, the R of TSV could be excessively large if there exists a serious resistive-open fault in TSV. As shown in Fig. 1(b), a resistive-open fault with a larger resistance R_{fault} is assumed to be existed in the TSV [8, 10].

Fig. 1. TSV model, (a) fault free; (b) including resistive-open fault

Depending on the defect location, x , the TSV is divided into two segments, $[0, x]$ and $[x, 1]$. The $[0, x]$ segment can be modeled as a capacitor with scaled-down capacitance xC and the $[x, 1]$ segment can be modeled as R_{fault} connecting to a capacitor with capacitance of $(1-x)C$. Depending on the severity level of the resistive-open fault, R_{fault} could be varied from a few Ω to infinity [9, 10].

2.2 Test structure

Fig. 2 shows the designed pre-bond TSV test structure, which is also based on the principle that the oscillation period can be influenced by the resistor-capacitor parameters of TSVs [9, 10]. As shown in Fig. 2, without loss of generality to illustrate the functionality, the designed test structure consists of 10 TSVs, 10 TG sub-circuits, and multiple basic logic gates. The TG sub-circuit includes a tri-state buffer and a transfer gate with two transistors. Clearly, the tri-state buffer in the TG should be designed in accordance with the signal transmission direction of the corresponding TSV.

The designed test structure can support normal functional mode and test mode. Clearly, the control signals t and c can be set to 0s to support the normal functional mode. Meanwhile, the driving strength of the TSV can be enhanced by the tri-buffer of the TG in normal functional mode. To avoid disturbing the test function in test mode, the logic gates whose outputs are connected to functional I/Os of the test structure can be designed as tri-state logic. In the test mode, without loss of generality to explain the functionality of the test structure, we assume that the control signal ts are set to 1s and the control signal cs in TG2 to TG10 are set to 0s. Clearly, when $c1$ in TG1 is set to 0, we can obtain the oscillation period from the oscillator shown in Fig. 2. And when $c1$ is set to 1, the oscillation period with variation caused by the resistor-capacitor parameter of TSV1 can also be obtained. As a result, the resistor-capacitor parameter related to a specific TSV can be reflected by the oscillation period variation. One of the important advantages of the test structure is that the oscillation period variation relies solely on the resistor-

Fig. 2. Test structure

capacitor parameters of TSVs due to the same signal propagation path in different oscillations.

2.3 Test flow

Based on the designed test structure, Table I shows the test flow for detecting faulty TSVs. The test flow can be divided into $N + 1$ test steps considering that N TSVs are included in a test structure. Without loss of generality, test steps and their corresponding control values for testing 6 TSVs are shown in Table I to describe the test flow.

Table I. Test steps and control signals

	$C1$	$C2$	$C3$	$C4$	$C5$	$C6$	t	Period	Variation
Step0	0	0	0	0	0	0	1	$P0$	NA
Step1	1	0	0	0	0	0	1	$P1$	$V1 = (P1 - P0)$
Step2	1	1	0	0	0	0	1	$P2$	$V2 = (P2 - P1)$
Step3	1	1	1	0	0	0	1	$P3$	$V3 = (P3 - P2)$
Step4	1	1	1	1	0	0	1	$P4$	$V4 = (P4 - P3)$
Step5	1	1	1	1	1	0	1	$P5$	$V5 = (P5 - P4)$
Step6	1	1	1	1	1	1	1	$P6$	$V6 = (P6 - P5)$

In step0, by setting 0s to the control signal cs in all TGs, all the transfer gates in TGs can be turned off. Hence, the oscillation period, namely $P0$, can be calculated after oscillation. Clearly, in this case, the resistor-capacitor parameters of TSVs are prevented to influence the oscillation period. Then, in step1, the transfer gate in TG1 is turned on, hence the oscillation period, denoted by $P1$, would be varied due to the influence of TSV1. As a result, period variation, namely $V1$, can reflect the resistor-capacitor parameter of the TSV1. Likewise, by successively turning on the transfer gates in TGs from step2 to step6, the period variation between two oscillations generated in successive steps can be calculated respectively. Theoretically, these period variations are equal if there exists no faulty TSV. Consequently, the faulty TSV can be detected by recognizing the period variation that deviates from the normal value. Based on the test flow, on average, the number of oscillations required to test one TSV is approximately only one.

3 Experimental results and analysis

In the work, the designed test structure was implemented using a commercial 0.18 μm CMOS technology and simulated by HSPICE simulation tool. The lumped capacitance of a TSV is assumed to 100 fF. The time for each oscillation is set to 4995 ns. Three main experiments are conducted in this work to verify the effectiveness of the proposed pre-bond TSV test method.

3.1 Experiment 1

In the first experiment, to verify the test functionality of the proposed test scheme, we assume that there exists a resistive-open fault of 3000 Ω in TSV3 and TSV7 of the test structure shown in Fig. 2, respectively. The resistive-open faults in TSV3 and TSV7 are assumed to locate at $x = 0.5$ and $x = 0.2$ respectively.

Fig. 3. Period comparison between two successive test steps

Based on the TSV model and the test flow, Fig. 3 shows the oscillation periods obtained from the test steps. The period variations between two successive oscillations are also calculated and showed in Fig. 3. Clearly, the period variations induced by fault-free TSVs are basically equal with only small calculation error. However, the period variations induced by the faulty TSVs are distinctly deviated from the normal values, and smaller period variation can be brought when the fault location is closer to the top end of the TSV. Clearly, by analyzing the distribution of period variations, 10 TSVs in the test structure can be tested with 11 oscillations.

3.2 Experiment 2

Clearly, even for fault-free TSVs, the period variations would be influenced by process variations. In this experiment, we evaluate this influence by Monte Carlo simulation. In the simulation, the inter-die and intra-die gate length variations of the library standard cells are considered to have Gaussian distributions, denoted by $N(\mu_L, \sigma_1)$ and $N(\mu_L, \sigma_2)$ respectively. Moreover, the capacitance of TSV is also considered to have Gaussian distribution, denoted by $N(\mu_C, \sigma_C)$.

Fig. 4 shows the period variations according to the test steps in Table I and the test structure in Fig. 2, which are obtained from 100 Monte Carlo simulations considering that $3\sigma_1 = 5\%\mu_L$, $3\sigma_2 = 5\%\mu_L$, and $3\sigma_C = 5\%\mu_C$. In reality, the period variation distribution can naturally be obtained by gathering period variation statistics when testing a batch of chips. Considering the process variations, the TSV with resistive-open fault, which induces a period variation even smaller than the minimum of that in the normal distribution, about 250 ps in Fig. 4, can be detected.

Fig. 4. Monte Carlo simulation of period variations

3.3 Experiment 3

Fig. 5 shows the minimum detectable resistances of resistive-open fault in TSV at the location from $x = 0.1$ to $x = 0.7$, by setting the detectable period variation to 250 ps and even more conservatively to 220 ps. The minimum detectable resistance is increased with the fault location gradually departing from the top end of the TSV. With the detectable period variation set to 250 ps and 220 ps, the minimum detectable resistances are about $500\ \Omega$ and $800\ \Omega$ at the location $x = 0.1$ and increase to $5000\ \Omega$ and $27500\ \Omega$ at the location $x = 0.7$ respectively.

Fig. 5. The minimum detectable resistances

As similar to all pre-bond TSV test methods, the resistive-open fault at the bottom of the TSV cannot be detected [9, 10]. Moreover, due to process variations, the detectable resistances of resistive-open faults occurred near the bottom locations of TSV, such as $x = 0.8$ and $x = 0.9$, are very large or even cannot be detected, thus are not shown in Fig. 5. On the whole, the proposed pre-bond TSV test scheme has a strong ability for quick resistive-open fault detection.

4 Conclusion

In this paper, we proposed an effective pre-bond TSV test scheme, including the test structure and flow. The test structure can provide high test accuracy due to the same signal propagation path in different oscillations. The number of oscillations is only $N + 1$ when testing N TSVs. Experimental results obtained from HSPICE simulation tool demonstrate that the proposed test scheme is effective.

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