Design of power efficient stable 1-bit full adder circuit

Shahmini Subramaniam, Ajay Kumar Singh,
and Gajula Ramana Murthy

*Digital VLSI Design Research Group, Faculty of Engineering and Technology,
Multimedia University, Jalan Ayer Keroh Lama, 75450 Melaka, Malaysia*

Abstract: This paper presents design of 14-T 1-bit full adder power efficient Pass Transistor Logic (PTL) based stable circuit. Due to compact architecture, power consumption is low and response is faster. MC (Monte Carlo) shows that the circuit is more reliable against any statistical variations.

Keywords: power efficient, Pass Transistor Logic (PTL), 1-bit full adder circuit, MC (Monte Carlo) simulations, reliability

Classification: Integrated circuits

References

- [1] Ch. Saraswathi, *et al.*: “High performance and energy efficient FinFET based 1-bit PT full adders,” *IEEE I. C. Computational Intelligence and Computing Research* (2016) 1 (DOI: [10.1109/ICCIC.2016.7919605](https://doi.org/10.1109/ICCIC.2016.7919605)).
- [2] A. Roohi, *et al.*: “Voltage-based concatenatable full adder using spin hall effect switching,” *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **36** (2017) 2134 (DOI: [10.1109/TCAD.2017.2661800](https://doi.org/10.1109/TCAD.2017.2661800)).
- [3] A. A. Tahrim, *et al.*: “Design and Performance Analysis of 1-Bit FinFET Full Adder Cells for Subthreshold Region at 16nm Process Technology,” *J. Nanomaterials* **2015** (2015) 726175 (DOI: [10.1155/2015/726175](https://doi.org/10.1155/2015/726175)).
- [4] I. Obridko and R. Ginosar: “Minimal energy asynchronous dynamic adders,” *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **14** (2006) 1043 (DOI: [10.1109/TVLSI.2006.884056](https://doi.org/10.1109/TVLSI.2006.884056)).
- [5] K. Purnima, *et al.*: “Design of modified shannon based full adder cell using PTL logic for low power applications,” *IJCSIT* **3** (2012) 2964.
- [6] K. R. Kumar, *et al.*: “Design of 2T XOR gate based full adder using GDI technique,” *IEEE I. C. on Innovative Mechanisms for Industry Applications* (2017) 10 (DOI: [10.1109/ICIMIA.2017.7975590](https://doi.org/10.1109/ICIMIA.2017.7975590)).
- [7] Deepa and V. S. Kumar: “Analysis of energy efficient PTL based full adders using different nanometer technologies,” *IEEE I. C. Electronics and Communication Systems* (2015) 310 (DOI: [10.1109/ECS.2015.7124914](https://doi.org/10.1109/ECS.2015.7124914)).
- [8] Y.-B. Fang, *et al.*: “An all-n-type dynamic adder for ultra-low-leakage IoT devices,” *IEEE I. C. ASIC* (2017) 68 (DOI: [10.1109/ASICON.2017.8252413](https://doi.org/10.1109/ASICON.2017.8252413)).
- [9] K. S. Jitendra, *et al.*: “A new low-power full-adder cell for low voltage using CNTFETs,” *IEEE I. C. Electronics Comput. Artif. Intell.* (2017) 1 (DOI: [10.1109/ECAI.2017.8166425](https://doi.org/10.1109/ECAI.2017.8166425)).
- [10] G. K. Reddy: “Low power-area pass transistor logic based ALU design using low power full adder design,” *IEEE I. C. Intelligent Systems and Control* (2015) 1 (DOI: [10.1109/ISCO.2015.7282289](https://doi.org/10.1109/ISCO.2015.7282289)).
- [11] K. Nehru, *et al.*: “Design of low power ALU using 8T FA and PTL based MUX circuits,” *IEEE I. C. Advances in Engineering, Science and Management* (2012) 145.

- [12] A. K. Singh, *et al.*: “Low power and high performance single-ended sense amplifier,” J. Circuits Syst. Comput. **22** (2013) 1350062-1 (DOI: [10.1142/S021812661350062X](https://doi.org/10.1142/S021812661350062X)).

1 Introduction

Full adder is most crucial component in arithmetic logic unit (ALU) which is used in computers, processors, communication devices, etc. Various design methods are adopted by researchers to design full adder circuits [1, 2, 3, 4]. Shannon decomposition based technique [5] has been proposed for a power efficient full adder circuit. Number of transistors reduced in this design which results in area minimization and power consumption on the cost of processing complexity. 2T XOR gate based full adder using Gate Diffusion Input (GDI) technique has been proposed [6] to optimize the circuit performance. Full adder can be designed using CMOS logic, transmission gates, dynamic logic or pass transistor logic [7]. All-n-type ripple-carry adder was proposed with low leakage for IoT devices [8]. It is observed that with all-n-type RCA, parasitic effects is lesser which produce high speed and low current leakage. Design of CNTFET based full adder ripple carry adder (RCA) has been proposed in literature [9] on the cost of processing complexity. Recently, researches are focusing on full adder circuit based on PTL design due to reduced complexity and power efficiency [10, 11]. In this paper, PTL based full adder circuit is proposed. The circuit shows better stability in terms of statistical variations and consumes lower power due to compact architecture. Due to lesser number of transistors, the response of the circuit is faster.

2 Architecture and layout of the proposed circuit

The proposed circuit is designed based on simplified Boolean expression to reduce the number transistors count. Fig. 1 shows the architecture of the proposed adder circuit. Inverters are introduced to generate the complement of inputs. The circuit is implemented in such a way that for each logic combination of inputs A, B and C in (C), 3 transistors turned ON and 3 turned OFF to reduce the power and delay. Let us consider following cases (Fig. 1); Case1: $A = 0$, $B = 0$ and $C = 0$, transistors N1, N4 and N6 turned ON whereas transistors N2, N3 and N5 turned OFF. The ON transistor N3 passes the logic B at the SUM node CARRY node. Case 2: $A = 0$, $B = 0$ and $C = 1$; transistors N2, N4 and N3 turn ON whereas N1, N5 and N6 are turned OFF. The ON transistor N4 passes high logic at SUM node and N3 passes low logic at CARRY. Case3: $A = 1$, $B = 1$ and $C = 0$. The ON transistor N5 passes the complement of B at SUM and ON transistor N3 passes logic A to CARRY. The layout of proposed adder is drawn using Microwind EDA tools for 45 nm technology (Fig. 2).

Fig. 1. Architecture of proposed adder

Fig. 2. Layout design of proposed adder

Fig. 3. Block diagram of 4-bit full adder & sense amplifier

3 Results and discussion

Table I and Table II give the logic level at SUM and CARRY nodes for various input combinations for various adder circuits. It is observed that the proposed adder circuit gives either strong high or strong low logic at SUM and CARRY nodes compared to the other circuits except for 101 inputs. We have implemented 4-bit series adder circuit (block diagram shown in Fig. 3) and observed that correct logic is obtained at two nodes for all the inputs combinations except 101 and 110 case. Since, in 4-bit series adder circuit, carry signal of first adder acts as input for the second adder and so on, it is observed that due to weak controlling signal at the gate of transistor N3, CARRY output degraded from 0.698 V to 0 V which can be

restored by using sense amplifier (SA) [12] or using low threshold voltage transistors N3 and N4. SA restores the output voltage swing and provides the appropriate output current to drive the fan-out capacitances whereas reduction in threshold voltages of the PTL transistors improves performance without increase in leakage current as in static CMOS logic.

Table I. Voltage output at sum node for 8 logic combinations

LOGIC	VOLTAGE SUM NODE (V)			
	PROPOSED 14T	REFERENCE [1]	REFERENCE [2]	REFERENCE [3]
0 0 0	0.000	0.000	0.242	0.000
0 0 1	0.814	0.681	0.845	0.139
0 1 0	0.814	0.716	0.621	0.931
0 1 1	0.000	0.000	0.000	0.000
1 0 0	0.839	0.716	0.793	0.501
1 0 1	0.000	0.000	0.000	0.000
1 1 0	0.000	0.000	0.294	0.260
1 1 1	0.839	0.690	0.966	0.578

Table II. Voltage output at carry node for 8 logic combinations

LOGIC	VOLTAGE CARRY NODE (V)			
	PROPOSED 14T	REFERENCE [1]	REFERENCE [2]	REFERENCE [3]
0 0 0	0.000	0.000	0.000	0.000
0 0 1	0.000	0.000	0.261	0.000
0 1 0	0.000	0.000	0.000	0.000
0 1 1	0.839	0.750	0.974	0.475
1 0 0	0.000	0.000	0.000	0.303
1 0 1	0.698	0.725	0.871	0.561
1 1 0	0.777	0.518	0.854	0.974
1 1 1	0.916	0.535	0.991	0.974

Lower leakage current in proposed adder is due to less number of OFF transistors at one time (Fig. 4). Monte Carlo (MC) simulations are performed on the proposed cell for 5000 samples for input combinations 111 and 101 (worst case scenario). The results have been collected in terms of voltage at SUM and CARRY nodes. Fig. 5(a) shows that the voltage at SUM node varies in between 0.839 V to 0.850 V with average of 0.845 V and standard deviation of 0.0032. Similar, observation is observed for CARRY (Fig. 5(b)) with average 0.922 V and standard deviation of 0.0077. For inputs 101, standard deviation of 0.001 and average 0.698 V are obtained (Fig. 6) for CARRY voltage whereas SUM output strongly maintains at 0. The MC simulation results show the robustness of the proposed adder circuit against statistical variation. MC simulation for 4-bit series adder circuit ($A = 1$, $B = 0$ and $C = 1$) gives average voltage variation from 0.701 V to 0 V at CARRY node and standard deviation from 0.003 to 0. Average power dissipation of $0.3 \mu\text{W}$

is observed for $A = B = C = 1$ (Fig. 7). For 101 inputs, power average is $0.849 \mu\text{W}$ (std. deviation = 0.002). The MC simulation results for 4-bit series adder circuit in case of 101 shows that average power consumption is 0.104 mW (standard deviation 0.003). These results predict the effectiveness of the proposed circuit against statistical variation. The proposed adder controls the leakage current effectively (Fig. 8) and gives faster response (Fig. 9).

Fig. 4. Power dissipation vs temperature analysis

Fig. 5. (a). Monte Carlo for voltage at sum node (logic 111)
(b). Monte Carlo for voltage at carry node (logic 111)

Fig. 6. Monte Carlo for voltage at carry node (logic 101)

Fig. 7. Monte Carlo for power dissipation at logic 111

Fig. 8. NMOS mode analysis: Power dissipation at logic 111

Fig. 9. Delay comparison

4 Conclusion

Due to compact architecture of the proposed circuit, leakage current controls effectively which results in lower power consumption. Due to absence of critical path in the circuit, response is faster. Monte Carlo simulations show that the proposed circuit is more reliable against any statistical variation. The proposed adder is able to attain strong low or high logic at respective node.