A $-86.88$ dBc/Hz @1 MHz K-band fractional-N frequency synthesizer in 90-nm CMOS technology

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Abstract: Through 90-nm CMOS technology, a K-band fractional-N frequency synthesizer has been designed. This paper proposes a new analysis to evaluate the noise current of the charge pump in fractional-N frequency synthesizer. It also designs an improved charge pump (CP). In addition, it also presents the multi-modulus divider (MMD) by the retiming technique. The measured phase noise achieves $-93.5$ dBc/Hz and $-86.88$ dBc/Hz for integer-N and fractional-N modes at 1 MHz offset, respectively. The in-band phase noise performance can be improved about 20 dB by the retiming technique. $-54.63$ dBc and $-50.7$ dBc reference spurs are respectively revealed by the spectrum for integer-N and fractional-N modes.

Keywords: frequency synthesizer, phase noise, charge pump, MMD, retiming technique

Classification: Integrated circuits
1 Introduction

In radio-frequency (RF) systems, it is widely recognized that the frequency synthesizer is a major building block for wireless communication and data communication. Generally, people utilize the fractional-N frequency synthesizer to generate the clean carrier for mixer, thus converting the data up or down to meet the desired frequency. As a result, commonly the frequency synthesizer are required to exhibit an excellent phase noise performance, thus avoiding corrupting signals in RF systems [1]. The noise from charge pump (CP) has a direct impact on the
frequency synthesizer output phase noise. As a result, the transceiver performance will be severely deteriorated [2]. Hence, low-noise charge pump is crucial for the production of local oscillator signal with high quality.

Literature has widely studied the charge pump for a long period. There are lots of researches on the improvement of the CP performance [2, 3, 4, 5, 6]. Researchers adopt a mismatch compensation loop, so as to mitigate the problem of the CP current mismatch for a wide range in Ref [3]. The channel-length modulation can be suppressed by a replica technique [4]. These studies put forward to various methods for CP, so as to reduce the CP current mismatch. On the contrary, previous literature focus little attention on the CP phase noise performance [2]. In addition, power ripple and environment noise can be suppressed by the charge pump with full-differential structure. Therefore, the differential charge pump compared to the single-end structure is preferred [5, 6]. However, the common-mode feedback (CMFB) circuit is needed by the fully-differential structure. It is worth noting that the noise current from the CMFB circuit has significant impact on the charge pump noise in the fractional-N mode and cannot think to be the common-mode (CM) noise. Previous studies usually neglect this point.

As we all know, the sigma-delta (SD) modulation method could shape the quantization noise of sigma-delta into high frequency [7]. However, it is usually neglected by past researchers that the quantization noise shaped to high frequency would be modulated to low frequency due to the nonlinear divider. Furthermore, since the noise transfer function of SD in the loop is low pass, the quantization noise modulated to low frequency noise couldn’t be removed, which would severely deteriorate the in-band phase noise of frequency synthesizer. Therefore, a linear multi-modulus divider (MMD) is also important in fractional-N frequency synthesizer.

This work implements a high performance K-band fractional-N frequency synthesizer in 90-nm CMOS technology. It then demonstrates and analyzes the CP noise contributed by the CMFB circuit. Based on the analysis, it proposes and verifies an improved charge pump applied in fractional-N frequency synthesizer. Besides, it also designs the MMD with the retiming technique. The measured spectrum reveals $-54.63 \text{ dBc}$ and $-50.7 \text{ dBc}$ reference spurs for integer-N and fractional-N modes, respectively. The measured phase noise for integer-N and fractional-N modes could achieve $-93.5 \text{ dBc/Hz}$ and $-86.88 \text{ dBc/Hz}$ at 1 MHz offset, respectively. What’s more, with the retiming technique, the in-band phase noise performance of frequency synthesizer could be improved about 20 dB.

2 Circuit realization of frequency synthesizer

Fig. 1 depicts the architecture of the proposed frequency synthesizer, which consists of a phase frequency detector (PFD), a charge pump, a low-pass filter (LPF), a LC-tank VCO, an output buffer, a divider chain and a sigma-delta modulator (SDM). The frequency synthesizer is a type-II fourth-order loop. The oscillation frequency of VCO achieves about 25 GHz and an output buffer is employed to match the impedance of ground-signal-signal-ground (GSSG) pads, thus facilitating the probe station measurement. The output of VCO is firstly
divided by a divide-by-16 prescaler and then the prescaler output is fed into the multi-modulus divider (MMD). The division ratio of MMD is controlled by a third-order sigma-delta modulator. The divider signal is fed back to the PFD to be compared with the reference clock. The comparison result controls the CP, so as to generate the control voltage for VCO through the third-order low-pass filter. In order to suppress the quantization noise of SDM, the loop bandwidth frequency is designed to be about 400 kHz.

Fig. 1. Proposed K-band fractional-N frequency synthesizer architecture.

3 Charge pump

Fig. 2 illustrates the schematic of the proposed charge pump. Cascode devices are adopted on the current sources, so as to suppress the effect of channel-length modulation on minimal up or down current variation over the desired charge pump output range [8]. Here, an operational amplifier (A) within a large output voltage range is employed to reduce the charge sharing effect [9]. The charge pump

Fig. 2. Schematic of proposed charge pump.
switches are made of complementary MOS transistors to ensure same rising and falling times [2].

The proposed CMFB circuit compares the output common-mode voltage with the reference voltage $V_{ref}$ and adjusts the charge pump current until $I_{up}$ is equal to $I_{down}$. The schematic of CMFB is shown in right part of Fig. 2. Assume $M_9 = M_{10}$, $M_{11} = M_{12}$ and $M_{13} = M_{14}$, then $I_1 = 2I_2$. Moreover, since $I_{down} = \beta I_2$, $I_{up} = aI_2$ and $\beta = 2a$, then $I_{up} = I_{down}$. Where $a = (W/L)_{1,2}/(W/L)_{15}$ and $\beta = (W/L)_{5,6}/(W/L)_{13,14}$.

It is well known that if the integer-N frequency synthesizer locks, the CP only works in the dead zone state. Nevertheless, the CP would work in charge or discharge state rather than dead zone state in the fractional mode. As a result, the noise from the CMFB circuit shouldn’t be neglected. Assume the CP works in the discharge state, the Noise current $i_{n2}$ and $i_{n5}$ represent the $M_2$ and $M_5$ noise current and can be expressed as [9]:

\[
i^2_{n2} = 4kTg_{m2} + \frac{K_p}{C_{ox}(WL)_2} \cdot \frac{g^2_{m2}}{f} \tag{1}
\]

\[
i^2_{n5} = 4kTg_{m5} + \frac{K_N}{C_{ox}(WL)_5} \cdot \frac{g^2_{m5}}{f} + v^2_{CMFB} \cdot g^2_{m5} \tag{2}
\]

In (1) and (2), the first term denotes thermal noise and the second term denotes flicker noise. The $v_{n,CMFB}$ in (2) represents the noise voltage of the CMFB circuit. Due to $i_{n2}$ and $i_{n5}$ are uncorrelated noise, the CP noise current $i_{n,CP}$ can be expressed as:

\[
i^2_{n,CP} = i^2_{n5} \times DN^2(t) + i^2_{n2} \times UP^2(t) \tag{3}
\]

Where the $DN(t)$ pulse and $UP(t)$ pulse represent the control signals of switches. The noise current $i_{n2}$ and $i_{n5}$ are sampled out at $f$ Hz. Each sample lasts a period of $\Delta t$. The spectrum of $UP(t)$ and $DN(t)$ can be calculated as [10]:

\[
S_{UP}(f) = S_{DN}(f) = \Delta t \text{sinc}(\pi f \Delta t) \tag{4}
\]

The spectrum of $i_{n2}$ and $i_{n5}$ are:

\[
S_{i_{n2}}(f) = i^2_{n2} \cdot 2\pi\delta(f) \tag{5}
\]

\[
S_{i_{n5}}(f) = i^2_{n5} \cdot 2\pi\delta(f) \tag{6}
\]

According to the convolution property [10], the CP noise current $S_{i,CP}$ can be derived into following:

\[
S_{i,CP}(f) = \frac{S_{DN}(f) \ast S_{i_{n2}}(f)}{2\pi} + \frac{S_{UP}(f) \ast S_{i_{n5}}(f)}{2\pi}
= \left(4kTg_{m5} + \frac{K_N}{C_{ox}(WL)_5} \cdot \frac{g^2_{m5}}{f} + 4kTg_{m2} + \frac{K_p}{C_{ox}(WL)_2} \cdot \frac{g^2_{m2}}{f}\right) \cdot \Delta t \text{sinc}(\pi f \Delta t)
+ (v_{n,CMFB}g_{m5})^2 \cdot \Delta t \text{sinc}(\pi f \Delta t) \tag{7}
\]

It is primarily because that the third-order single-loop SDM is employed, the maximum division ratio variation of MMD is two [7]. Moreover, since the division ratio of prescaler is 16 in this work, the maximum phase error $\Delta t_{\text{max}}$ is about $16 \times 2T_{\text{vco}}$, where the $T_{\text{vco}}$ represents the period of the VCO output. Then the maximum noise current $S_{i,CP}$ can be simplified as below:

\[
S_{i,CP}(f) = \left(4kTg_{m5} + \frac{K_N}{C_{ox}(WL)_5} \cdot \frac{g^2_{m5}}{f} + 4kTg_{m2} + \frac{K_p}{C_{ox}(WL)_2} \cdot \frac{g^2_{m2}}{f}\right) \cdot 32 \cdot \Delta t \text{sinc}(\pi f \Delta t)
+ (v_{n,CMFB}g_{m5})^2 \cdot 32 \cdot \Delta t \text{sinc}(\pi f \Delta t) \tag{8}
\]
\[ S_{\text{cp}}(f) = \left( 4kTg_{m5} + \frac{K_N}{C_{\text{ox}}(WL)_5} \cdot f \cdot g_{m9}^2 + 4kTg_{m2} + \frac{K_P}{C_{\text{ox}}(WL)_2} \cdot f \cdot g_{m2}^2 \right) \cdot \Delta t \text{sinc}(32\pi T_{\text{vco}} f) + (v_{n,\text{CMFB}} g_{m5})^2 \cdot \Delta t \text{sinc}(32\pi T_{\text{vco}} f) \] (8)

The first term in (8) represents the noise of current sources and the second term in (8) represents the noise contributed by CMFB circuit. From the above equation, it is worth noting that reducing \( g_{m2,5} \) and \( v_{n,\text{CMFB}} \) can effectively improve the noise performance. As illustrated in Fig. 3, the simulation reveals that \( g_{m5,6} \) changes proportionally with \( S_{\text{cp}} \).

The \( i_{n,\text{CMFB}} \) represents the noise current from the CMFB circuit and can be written as:

\[ i_{n,\text{CMFB}}^2 = 4kTg_{m9,10} + 4kTg_{m13,14} + \frac{K_P}{C_{\text{ox}}(WL)_{9,10}} \cdot f \cdot g_{m9,10}^2 + \frac{K_N}{C_{\text{ox}}(WL)_{9,10}} \cdot f \cdot g_{m13,14}^2 \] (9)

Where \( k = 1.38 \times 10^{-23} \) J/K is the Boltzmann constant. Since the output impedance of CMFB circuit is \( 1/g_{m13,14} \), then \( v_{n,\text{CMFB}} \) can be calculated as:

\[ v_{n,\text{CMFB}}^2 = 4kT \frac{g_{m9,10}}{g_{m13,14}} + 4kT \frac{1}{g_{m13,14}} + \frac{K_P}{C_{\text{ox}}(WL)_{9,10}} \cdot f \cdot g_{m9,10}^2 + \frac{K_N}{C_{\text{ox}}(WL)_{9,10}} \cdot f \cdot g_{m13,14}^2 \] (10)

It could be seen from (10) that the noise is positively related to \( g_{m9,10} \); and the simulation in Fig. 4 implies that \( S_{\text{cp}} \) degrades as \( g_{m9,10} \) increases.

### 4 VCO

The \( K \)-band VCO, whose schematic is depicted in Fig. 5, employs ac coupling capacitors with a terminal biased with \( VDD/2 \) so as to increase the frequency of tuning range [11]. The fully differential tuning range technique is utilized to reject the common-mode interference and improve the phase noise performance [12]. This paper utilizes the filter method to suppress the noise of bias current, which is also beneficial to the phase noise performance [12, 13, 14]. To achieve a small
VCO gain $K_{\text{vco}}$, a 4-bit digital-controlled capacitor array is employed for coarse frequency tuning; and a varactor is utilized for fine frequency tuning [11, 12, 13, 14, 15]. A 2-bit tunable tail current source is also applied, in order to increase the VCO loop gain and enhance the phase noise performance [11, 16].

Fig. 4. Simulated the noise current of charge pump $S_{\text{cp}}$ versus $g_{m9,10}$.

5 MMD

The MMD, whose division range is 32–39, is composed of a 4/5 divider, an $S$ counter and a $P$ counter. As illustrated in Fig. 6, the $DFF0–DFF4$ forms the $P$ counter. It begins to inversely count from the code 11111 until the desired count is obtained. Then the OVER signal would change to low level and reset $P$ counter and $S$ counter. Meanwhile, $P$ counter is reset to 00000. After the next input code is detected, the OVER signal would change to a high level again.

The critical time sequence of the $P$ counter is depicted in Fig. 7. $T_{\text{ckq}}$ denotes the delay time of D flip-flop (DFF). $T_{\text{ecq}}$ represents the delay time of the detect circuit. $T_{\text{rs}}$ represents the delay time of DFF reset. Assume the 00010 and the 11111 respectively denote the final code and the initial code. As illustrated in the upper half part of Fig. 7, the time sequence reveals that width of the final code 00010 is equal to the sum of $T_{\text{ecq}}$ and $T_{\text{rs}}$; The $T_{\text{ecq}}$ wouldn’t be a constant as the divide ratio of MMD changes. Besides, the edge of MMD output clock aligns to the edge of...

Fig. 5. Detailed schematic of $K$-band VCO.
final code. Consequently, the rising edge of MMD output clock is also uncertain and nonlinear in the fractional-N mode. Hence, in-band phase noise performance may be seriously deteriorated. In order to solve this problem, the retiming circuit...
DFF5 is employed in the $P$ counter as shown in Fig. 6. Then the width of final code 00010 would be the sum of $T_{clk}$ and $T_{rs}$, as demonstrated in the bottom half part of Fig. 7. Where $T_{clk}$ denote the period of input clock which is a constant. The new time sequence reveals the output clock become more linear. The simulation in Fig. 8 reveals that the MMD without retiming technique output frequency wouldn’t be accurate as the divide ratio changes.

6 Experimental results and analysis

![Chip microphotograph](image)

Fig. 9. Chip microphotograph.

![Measured maximum and minimum locking frequencies for every VCO band](image)

Fig. 10. Measured maximum and minimum locking frequencies for every VCO band.

This experiment implements the $K$-band fractional-$N$ frequency synthesizer in TSMC 90 nm CMOS process. Fig. 9 shows that the chip micrograph of the proposed frequency synthesizer and the chip area is 1380 $\mu$m $\times$ 630 $\mu$m. The frequency synthesizer consumes 74 mW including the output buffer with a 1.2 V power supply. The measurement is performed on the probe station. The phase noise performance is measured using the Agilent N9030B Spectrum analyzer and the reference clock is generated by Agilent 8257D signal generator. Serial peripheral interface (SPI) provides digital control signal from the host computer to control codes of each module.

As illustrated in Fig. 10, the measured locking range of the VCO is 22.7 GHz to 28.6 GHz. Fig. 11 reveals that $-54.63$ dBc and $-50.7$ dBc reference spurs at 45 MHz offset for integer-$N$ and fractional-$N$ modes, respectively. As seen from
Fig. 12, the phase noise could achieve $-93.5$ dBc/Hz and $-86.88$ dBc/Hz at 1 MHz offset for integer-N and fractional-N modes, respectively. Fig. 12 also shows that the in-band phase noise performance can be improved about 20 dB with the retime technique. Table I provides a summary of the $K$-band fractional-N frequency synthesizer performance compared with the state-of-the-art frequency synthesizers. It provides promising potential for low-noise designs in RF systems.
Table I. Comparison with the state-of-the-art frequency synthesizers

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<tr>
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<th>This work</th>
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<th>[18]</th>
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<td>-26</td>
<td>-28</td>
<td>-32</td>
<td>-26.7</td>
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<td>Output clock (GHz)</td>
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<td>0.8 V</td>
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*Normalized to 45 MHz reference: PN (dBc/Hz) + 20 log(f_ref/45 MHz) [20]

7 Conclusion

A high performance K-band fractional-N frequency synthesizer was proposed in this study. In the proposed frequency synthesizer, a new analysis to evaluate the noise of the charge pump in the fractional-N frequency synthesizer was demonstrated and analyzed. Based on this analysis, this paper presented an improved charge pump. Besides, the design methods of K-band VCO were presented. In addition, the MMD with retime technique is designed in order to enhance the in-band phase noise performance. The measured reference spurs were $-54.63$ dBc and $-50.7$ dBc for integer-N and fractional-N modes, respectively. The measured phase noise respectively achieved $-93.5$ dBc/Hz and $-86.88$ dBc at 1 MHz offset. With the retime technique, the in-band phase noise performance could be optimized about 20 dB. Measurement results were also compared with the works published over the past decade, indicating that the proposed frequency synthesizer achieved an excellent performance.

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