A novel highly reliable and low-power radiation hardened SRAM bit-cell design

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Abstract: In this paper, an improved SEU hardened SRAM bit-cell, based on the SEU physics mechanism and reasonable circuit-design, is proposed. The proposed SRAM cell can offer differential read operation for robust sensing. By using 90 nm standard digital CMOS technology, the simulation results show that the SRAM cell can provide full immunity for single node upset and multiple-node upset. And its critical charge is 25 times compared with Quatro10T. Besides, by comparing several electrical parameters, the proposed SRAM cell has the highly reliable and low-power capability for severe radiation environment application.

Keywords: single event upset, radiation hardened SRAM cell (RHSC), multiple-node upset, static random access memory (SRAM)

Classification: Integrated circuits

References


1 Introduction

Static Random Access Memories (SRAMs) are widely used in digital information processing and control system, because SRAMs has some good features such as high integration, fast storage speed, and fully compatible with CMOS process. In space exploration and high energy physics experiment, SRAM needs to work long hours in a high dose of radiation environment, which can be affected by radiation strikes, such as cosmic rays and alpha particles. If these radiation particles hit the sensitive nodes of SRAM cells, a SEU (single event upset) occurs because of enough charge collection at the sensitive nodes [1]. The SEU can change the stored data of the SRAMs which will lead to system function disorder and cause serious consequences. Moreover, the scaling down CMOS technology has made a bad effect on SRAM cells in radiation resistance because of lower supply voltage and smaller feature size of transistors [2]. Therefore, it is necessary to study and design SRAM cell that has the ability of resisting SEU [3].

Up till present, lots of radiation hardened SRAM cells have been proposed to mitigate SEU effect. An example of a widely used hardening design has been reported in [4] which commonly known as DICE. The DICE memory cell uses conjoint transistors to provide complete SEU fault immunity for every single node. Besides, the DICE design does not need to enlarge the size of transistors. Due to charge sharing, when the sensitive nodes of conjoint transistors are stroked by radiation particles, the stored data of DICE will be changed. So it can not tolerant multiple-node upset. In Fig. 1(a), a 10 T hardened SRAM cell using ten transistors is proposed, which is named as Quatro10T cell [5]. This design may cause less power. However, it can only recover from 1 \rightarrow 0 SEU. In Fig. 1(b), a proposed 10 T uses the inserting transistors to improve the robustness for SEU [6]. The increased transistors are working like resistance because of being in linear region,
which restrict the feedback path. Moreover, with the development of CMOS process technology scaling, the influences of single event multiple-node upsets because of charge sharing are becoming more severe [7, 8]. So, more reliable memory designs have to be considered. In [9] a new 13 T SRAM cell structure is proposed as shown in Fig. 1(c), and it takes superiority of hysteresis effect of Schmitt trigger to tolerate the multiple-node upset on the basis of the structure of 11 T [10] which can improve reliability of the cell. But generating higher power consumption and occupying more layout area are the main disadvantage of the 13 T SRAM cell, and the single-ended structure is not common for commercial use.

In this paper, a novel SEU robust SRAM cell (RHSC-12T) is proposed. With the help of smart circuit design, the proposed SRAM can provide full immunity for single node upset and multiple-node upsets with highly reliable and low-power performance.

2 Proposed SEU robust SRAM cell circuit design

The proposed SEU tolerant SRAM cell circuit (namely RHSC-12T) is shown in Fig. 1(d). On the basic of Quatro10T in [5], two NMOS transistors are added to prevent a 0 → 1 SEU happening at node Q or QN. This improvement can improve the SEU robustness. Two access transistors, N3 and N4, connect the bit lines (BL...
and BLN) with the storage nodes Q and QN. Besides, cross coupled transistors pairs P3∼P4 are also the storage nodes, which create the redundancy of data for SEU tolerant.

Now, operational principle of the proposed SRAM cell is introduced. Suppose the stored data is \(1(Q = 1, QN = 0)\) for the proposed RHSC-12T. First, the proposed SRAM cell is in the hold state, when word line WL is set to 0, transistors N3 and N4 are turned off. Transistors N1, N6, N8, P2 and P4 are turned off, while other transistors are turned on. The proposed SRAM cell easily maintains its initial state. During the read operation, the bit-lines are pre-charged to 1 state by the pre-charge module, when the word-line is set to 1 state, the read operation begins. The state of node Q remains unchanged, but the voltage of the BLN starts to drop through the driven transistors N2 and N4. Then, the small voltage difference happens between the bit-lines. When the difference is big enough, a sense amplifier monitors the difference and passes the stored state to the output. At last, to change the stored data of the proposed SRAM cell, the word-line WL is set to 1. Then the BLN is pre-charged to VDD, the BL is pulled down to 0 simultaneously. As a result, the state of QN is charged to 1 by BLN, which turns on the transistors N1 and N6. Then, the state of nodes Q and S1 are discharged to 0 because of the opened NMOS N1 and N6. Finally the transistor P4 is turned on by the S1, and the S0 is pulled up to 1. The write operation is done.

The SEU recovery analysis is introduced as follows. Considering the state shown in Fig. 1(d) we can find that the nodes S0, S1 and Q are easily affected by radiation particles because these nodes of the cell are surrounded by the reverse-biased drain junctions of a transistor biased in the OFF state [11]. Node QN is not affected by radiation particles because the state of QN is 0, and QN is only surrounded by NMOS transistors. On the basis of SEU physics mechanism, when a heavy ion hits NMOS transistors around QN, only a negative transient pulse occurs which will not change the state of QN. The SEU robustness of the proposed RHSC-12T is discussed detailedly.

1) If state of node Q is changed by radiation particle, it goes low state and turns on transistor P2. Transistors N2 and N5 are turned off because of the 0 state of node Q, which makes the nodes QN and S0 in a high impedance state. But, node QN and S0 hold their original state 0, and node S1 keeps original state 1. Then the node Q is pulled to VDD through the transistors P1 and N7, because transistors P1 and N7 are still on. Then transistors N2 and N5 are turned on again.

2) If node S0 is stuck by radiation particle, it goes high and turns off the transistor P3. At the same time, the N8 is turned on because of the change of the node S0. The disturbance of node S0 cannot be propagated to node Q. Node Q holds its original 1 state, which makes the transistor P2 be still off. Thus, the path between node QN and VDD is closed. The state of QN is not changed, and the node S0 is discharged to 0 through the opened transistors N5.

3) If the stored data in node S1 is changed to 0 by heavy ion, it will turn on the transistor P4 and turn off transistor N7. Then S0 is pulled up to 1 by VDD which turns on transistors N8, then node Q is in a high impedance. Due to the capacitive effect, node Q does not change its original 1 state immediately, which makes the transistors N2 and P2 be ON state and OFF state respectively. Thus node QN is not
changed to 1 state because of the closed transistor P2. Transistor N5 remains ON state because node Q maintains original state 1. At this time, N5 and P4 are opened simultaneously, so S0 may be in an uncertain state. In order to pull down the voltage of S0, we appropriately enlarge the size of N5, which can enhance the driverbility of N5 and the node S0 is discharged from 1 to 0 through transistor N5 finally. The result is that transistor P3 is turned ON again, node S1 is pulled up to original high state by VDD. At last, transistor N7 is turned on and transistor N8 is shut off again, and the cell recovers its initial state successfully.

4) Due to charge sharing effect, if pair nodes are hit by a particle radiation, the S0 and S1 will be flipped simultaneously, which is named as multiple-node upsets. The transistor N7 is turned off, which makes node Q in a high impedance state, but it does not change its initial 1 state. Although transistor N8 is turned on by the changed S0, the transistors P2 and N2 controlled by node Q are still OFF and ON state. So QN maintains its original 0 state. At last, nodes S0 can recover its initial 0 state because of the opened transistor N5, which can help node S1 recharged to VDD. Thus the initial stored data of the proposed RHSC-12T is maintained.

From the above analysis, if any sensitive node such as S0, S1, Q or a pair node S1–S0 is hit by heavy ion, the transient voltage fluctuation perturbation can’t be propagated to the hold cell. After soon, the cell can recover its original state. Therefore, the proposed SRAM cell is highly reliable for severe radiation environment application.

3 Evaluation

The simulations are done with the simulation tool Cadence Spectre. By using 90 nm standard digital CMOS technology, we set the simulation parameters at 1.2 V power supply and room temperature (25°C). For equity comparisons, all the SRAMs are designed by the same sizes.

To simulate a SEU caused by the particle injection, a double exponential current pulse is used [9, 11, 12]. In Fig. 2(a), to imitate a negative transient pulse, we add a current source connected to the drain terminal of the NMOS. In the same way, the same method is used in PMOS to imitate a positive transient pulse in 2(b).

![Fig. 2. Equivalent circuits used for simulation: (a) Negative transient pulse; (b) Positive transient pulse](image-url)
In the SEU simulation, the proposed cell stores 1 state (i.e., $S_1=1$, $S_0=0$, $Q=1$, $QN=0$) at the beginning. Subsequently, a double exponential current pulse ($I_{SET}$) injected into the sensitive nodes is used for mimicking a single event transient (SET). The value of current pulse is set to 0.39 mA to simulation a 100 fC particle-induced charge injection. When $I_{SET}$ is injected into the sensitive nodes $S_1$, $S_0$, and $Q$, the transient performance of the storage nodes $S_1$, $S_0$, and $Q$ are shown in the Fig. 3.

Simulated results show no flip happening in the memory cell for these sensitive nodes. At 22 ns, a $0 \rightarrow 1$ transient fault is occurred at $S_0$ when the $I_{SET}$ strikes node $S_0$. Then it takes 2 ns to recover to its initial state 0. Similarly, at 22 ns, when the $I_{SET}$ strikes node $Q$, a $1 \rightarrow 0$ transient fault is appeared at node $Q$. It just takes 1 ns to recover to its initial state 1. It is the same case when node $S_1$ is stroked by $I_{SET}$. Besides, at 22 ns, when the $I_{SET}$ hits pair nodes $S_0$–$S_1$, a $1 \rightarrow 0$ transient fault and a $0 \rightarrow 1$ transient fault are observed at nodes $S_1$ and $S_0$ simultaneously. Deservedly, the nodes $S_1$ and $S_0$ recover their original state 1 and 0 [12].
The performance of the proposed SRAM cell is compared with the standard 6 T cell, Quatro10T, 10 T, and 13 T cell [9]. The comparison parameters include the critical charge ($Q_{\text{crit}}$), transistors number, read access time, write access time, power consumption, and area. The $Q_{\text{crit}}$ is measured by the above-mentioned current injection way finding the least deposited charge amount which can make the cell upset [13]. Read access time is measured as the time interval from the active word line edge crossing its threshold (50% of VDD) to bit lines developing 50 mV differential voltage. Besides, to simulate a high fan-out in read operation, a 0.3 pF capacitance is added to bit-lines. Write access time which is defined as the time interval from the midpoint of active word line edge to the intersection of cell’s two storage nodes. The results of comparison parameters for various radiation hardened SRAM cells are shown in Fig. 4(a). And the simulation of $Q_{\text{crit}}$ is shown.

![Comparison of different SRAM cell](image1)

![Comparison of $Q_{\text{crit}}$](image2)

**Fig. 4.** (a) Comparison of different SRAM cell, (b) Comparison of $Q_{\text{crit}}$
in Fig. 4(b). The simulation results of comparison parameters in Fig. 4 have been normalized to 6 T memory cell.

Compared with the other hardened SRAM cells, the proposed SRAM cell not only has the largest critical charge, but has the lowest power consumption, which can be used in future low power aerospace applications. The read access time is almost the same as the standard 6T cell. Besides, the write access time is comparable among the various SRAM cells. Compared with the other hardened SRAM cells, the disadvantage is that the proposed SRAM cell has the 2nd area, because two NMOS transistors are added to prevent a $0 \rightarrow 1$ SEU happening at node Q or QN, which provides complete immunity for single node upset and multiple-node upset. After comparison with other hardened SRAM cells, the results reveal the proposed cell has the excellent capability for SEU fault-tolerant, and comparable electrical performances which makes it suitable for critical aerospace applications.

4 Conclusion

In this paper, an improved SRAM cell on the basis of Quatro10T with highly reliable and low-power capability is proposed. The proposed SRAM cell can offer differential read operation for robust sensing, which is critical for easier design of the sense amplifier and for reliable sense operation. The critical charge is 25 times larger than the Quatro10T, which is excellent and suitable for severe radiation environment applications. The simulation results show it can not only completely tolerate an SEU on any one of its internal single node, but provides multiple-node upsets protection for initial state of the cell. Besides, compared with other hardened SRAMs cells, the proposed SRAM cells has comparable or better performance in terms of $Q_{crit}$, read/write access time, area, and power consumption.