Capacitance multiplier with large multiplication factor, high accuracy, and low power and silicon area for floating applications

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Abstract: A capacitance multiplier with high accuracy and reduced power consumption and silicon area, is presented. It offers a scaling factor based on ratios of resistors that can be physically matched to reduce deviations due to fabrication process. Resistor ratios also offer the property to define large scaling factors without increasing power consumption or silicon area. It is based on a modified current-mode multiplication technique that scales voltage magnitude instead of internal devices of the current-providing device. Simulation results show scaling factors of 10, 100, 1 k and 10 k. Experimental testing shows the results of the implementation of the floating equivalent multiplier implemented in a notch RLC filter with a scaling factor of 1 k.

Keywords: analog integrated circuits, capacitance multipliers

Classification: Integrated circuits

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1 Introduction

Modern electronic implementations demand high level of integration where several functions are executed on a single chip. This represents a limitation for applications that require passive elements, specifically capacitors, which occupy large silicon area. Many topologies to increase the effective value of integrated capacitors have been proposed over the last few years; these can mainly be divided into two design strategies, voltage- and current-mode multipliers. The former utilizes voltage amplification between the two terminals of a capacitor by means of an active gain stage. Probably the most common example of this type of multiplication is the one used for frequency compensation in operational amplifiers (op-amp) with two (or more) gain stages, commonly known as the Miller compensation. Large multiplication factors are achieved with this method, as it typically depends on the gain of a common-source stage of the form $g_m r_o$, where g_m is the transconductance gain and r_o the output resistance of a transistor.

However, these parameters can be seriously affected by the fabrication process; therefore, poor accuracy is a considerable drawback for this technique. On the opposite side, the other type of multipliers, the current-mode multipliers, are based on a scaled replica of the current through a capacitor. This method is illustrated in Fig. 1a, where the current in the capacitor i_c is sensed, scaled by a factor k in a dependent current source, and sunk from the same node which results in an output current of $i_c(k + 1)$. This gives an equivalent capacitance of $C_{eq} = C(1 + k)$. Unfortunately, the multiplication factor is usually small, as power and silicon area are directly proportional to it. Several variations have been proposed; however, some of them rely on active parameter values that depend on fabrication process, such as those in [1] and [2], especially the latter, which also considers very small biasing currents of nA where the signal-to-noise ratio and slew rates are significantly affected, in addition to the increased effect of mismatched parameters. In [3], where the multiplication factor is defined electrically, the non idealities of the active devices represent an additional factor that considerably affects the accuracy of the multiplication.

Fig. 1. Current-mode capacitance multipliers showing a) basic operation, b) conventional practical implementation, c) implementation using differential amplifiers [4], d) proposed circuit with increased voltage amplitude for OTA2, and e) proposed floating implementation.

2 Conventional capacitance multipliers

Typically, scaled current mirrors are used to implement the aforementioned technique. Fig. 1b shows the most basic implementation, where proper layout techniques allow parameter matching between the transistors in the mirror, thus considerably increasing the accuracy. Here, the diode-connected transistor M1 senses the current in capacitor C, which is then mirrored by M2 by a scaling factor k , thus sinking an output current $i_c(k+1)$ which results in an effective capacitance of $C(k+1)$. Unfortunately, this implementation has considerable limitations; the most important one is that the power consumption and silicon area increase proportionally to the factor k . Also, at high frequencies where the impedance of the capacitor decreases, the signal is mounted on a dc level defined by the gate-source voltage of M1, V_{GS1} . To overcome this, a practical implementation using Operational Differential Amplifiers (OTA) was proposed in [4] and is shown in Fig. 1c. In this architecture, OTA1 senses the current in capacitor C, and OTA2, which has the same input voltages as OTA1, induces a current k times larger, thus having the same effect as the conventional multiplier. This solution offers the advantage of mounting the dc level of the signal to ground at high frequencies, however, it has the same other limitations than the conventional multiplier.

Other variations have been proposed in the past, such as that in [5], which offers an exponential multiplication factor with a reduced implementation by stacking current mirrors in series. However, it still has increased power consumption and mismatched parameters between devices are multiplied by the following scaling stages. Another implementation is that reported in [6], which describes a multiplier with a transresistive mode of operation; although it has a multiplication factor of the form g_m/R , where the transconductance gain g_m is still affected by the fabrication process.

3 Proposed capacitance multiplier

As previously discussed for the circuit in Fig. 1c, having the same input signals OTA2 provides currents k times larger than OTA1 given that it is internally scaled by the same proportion. However, another option for OTA2 to provide large currents is by scaling its input signals with respect to those for OTA1 instead of increasing the size of internal devices, which eliminates the need for large power consumption and silicon area.

The proposed circuit is shown in Fig. 1d, where a resistor R is included in the local feedback loop of OTA1. When a current i_c is present in the capacitor, it induces a voltage drop in the resistor of $V_R = i_c R$ which increases the amplitude of the signal fed to OTA2, and hence, the current it provides. This current can be defined as

$$i_{kc} = g_{m2} V_{o1} = g_{m2} (V_R - V_{i-1}) = i_c g_{m2} (R - 1/g_{m1}) \quad (1)$$

Where g_{m1} and g_{m2} are the transconductance gain of OTA1 and OTA2, respectively. Considering that $R \gg 1/g_{m1}$ this current results in $i_{kc} \approx i_c g_{m2} R$; note that the design of the gain g_{m2} involving active devices affects the accuracy by undesired non-idealities. Therefore, for accuracy purposes, it is optimal to consider a topology for OTA2 with a transconductance gain that depends on a resistor and is of the form $g_{m2} = k/R$. Thus, similar to the case of the conventional multiplier where matched transistors offer high accuracy, resistors here can be physically matched, offering a gain based on ratios rather than exact values that depend on non-desired deviations due to fabrication. Also, large ratios using resistors are possible without consuming additional power or excessive silicon area.

Before describing the design of OTA2, note that this approach corresponds to that of a grounded implementation; however, access to both terminals of the equivalent capacitor is desired for some applications. The differential inputs of the amplifiers offer the property to define the floating version of the multiplier, also proposed here and shown in Fig. 1e. Here, two grounded multipliers are used, where the grounded terminals of each of them is connected to the opposite terminal of the floating realization, thus, the currents induced in each capacitor C depend on the voltage defined at the two terminals of the multiplier.

As discussed earlier, OTA2 requires a gain that depends on a resistor, for which we may consider the basic operation shown in Fig. 2a. Here, two unity-gain buffers refer the differential input signals to resistor R_k ; the induced currents are then sensed and summed to the output node, which results in a transconductance gain of $g_m = i_o/V_i = 2/R_k$. One practical implementation of this scheme was reported in [7], where high performance voltage followers were considered for the implementation of the buffers. A brief description of its operation is as follows: it uses the follower reported in [8], denominated Folded Flipped Voltage Follower (FFVF), and shown in Fig. 2b. Here, transistor $M2$ has a constant bias current, hence it has a constant gate-source voltage, and reflects the input voltage at the output node level shifted by V_{GS1} , acting as the voltage following device. The local feedback allows $M1$ to adjust its gate-source voltage, so it offers the capability to source large currents, and it offers an output resistance of $\approx 1/g_{m1}g_{m2}r_{o2}$. It is similar to the popular Flipped Voltage Follower [9, 10] shown in Fig. 2c; however, the FFVF has

an increased output swing of $V_{DD} - V_{GS1} - 2V_{DSsat}$, compared to that of the FVF which is limited to $V_{TH} - V_{DSsat2}$.

Fig. 2. a) Basic operation of the resistor-based OTA, b) Folded Flipped Voltage Follower (FFVF) [8], c) Flipped Voltage Follower (FVF) [9], d) practical implementation of the resistor-based OTA [10], and e) conventional amplifier topology used for OTA1.

The Resistive-based OTA using the FFVF [7] is shown in Fig. 2d, which includes a resistor R_k , the voltage followers formed by transistors M1a, M2a and M1b, M2b, and the current mirrors formed by M3–M6. A differential voltage applied at the input terminals is referred to the resistor R by means of the voltage followers FFVF1 and FFVF2, the induced current $i_{Rk} = V_i/R_k$, is sourced by one of the followers and subtracted from the other, which is then mirrored to the output by means of M3–M6. This results in a transconductance gain of $i_o/V_i = 2/R_k$. An important aspect is that voltage following transistors M2a and M2b in the FFVFs is affected by the body effect just as a conventional common-drain voltage follower is, which has a gain different from unity and of the form $A_{vf} = g_m/(g_m + g_{mb})$. Hence, the gain of the OTA results in $g_m = 2A_{vf}/R_k$.

With this the multiplier in Fig. 1d has a current $i_{kc} = i_c g_{m2} R = i_c R (2A_{vf}/R_k)$, where the scaling factor is $k = 2A_{vf}R/R_k$, and the resistors can be scaled appropriately, and physically matched using layout techniques. The equivalent capacitance is $C_{eq} = C(k + 1) \approx kC$ for $k \gg 1$. As the floating implementation includes two capacitors, the gain factor results in $k = g_{m2}R/2 = R/R_k$. For OTA1 in Fig. 1d, the conventional OTA depicted in Fig. 2e was considered. Note that for values of $R \leq 1/g_{m1}$ the output voltage of OTA1, V_{o1} , maintains the same phase as its inverting input; however, for $R > 1/g_{m1}$, R causes an inversion in V_{o1} , therefore, the polarity of OTA2 must also be inverted in order to maintain negative feedback, as shown in Fig. 1d and 1e.

Frequency analysis

The frequency analysis of the multipliers is of interest to determine their operational range and behavior. The grounded version was considered for simplicity. Assuming that i_c and i_{kc} are the current in C and the output current from OTA2 respectively, small signal analysis shows that these currents are given by

$$i_c = v_o(sC) \left[\frac{1 + g_{m1}r_{o1}}{(1 + g_{m1}r_{o1}) - sC(r_{o1} + R)} \right] \quad (2)$$

$$i_{kc} = v_o \left[\frac{sCg_{m2}r_{o2}[r_{o1}(1 - g_{m1}R)] - sC(r_{o1} + R) + (1 + g_{m1}r_{o1})}{r_{o2}[(1 + g_{m1}r_{o1}) - sC(r_{o1} + R)]} \right] \quad (3)$$

Where r_{o1} and r_{o2} are the output resistances of OTA1 and OTA2, respectively. Considering that the total output current of the multiplier is defined as $i_o = i_c + i_{kc}$, working equations (2) and (3) in this relation we obtain the output impedance $Z_o = v_o/i_o$ –not included here due to limited space–, where v_o is the output voltage. This analysis shows one RHP zero and one LHP pole defined as:

$$\omega_z \approx \frac{g_{m1}r_{o1}}{C(R + r_{o1})}; \quad \omega_p \approx \frac{-g_{m1}r_{o1}}{C[g_{m2}r_{o2}g_{m1}r_{o1}R - (r_{o1} + R)]}$$

Which for $R > r_{o1}$ the pole results in $\omega_p = -1/RCg_{m2}r_{o2}$. The upper and lower operational limits known as Parallel Load Resistance (PLR) and Equivalent Series Resistance (ESR), found at low and high frequencies, have values of $\approx r_{o2}$ and $\approx (1 + k_x)/kg_{m1}$, respectively, assuming R is k_x times larger than r_{o1} for the latter.

Observe that large values of R results in the circuit having two high resistive nodes, the outputs of the amplifiers, which may introduce sufficient phase shift in the feedback loop to make the circuit susceptible to instability in frequency. In such case, a small compensating capacitor C_c may be included at the output of OTA1. To find the value of C_c , we consider the open-loop analysis, where the circuit shows a dc gain of $g_{m1}r_{o1}g_{m2}r_{o2}$, a dominant pole at $1/RC_c$, and a first non-dominant pole at $1/r_{o2}C_{o2}$ where C_{o2} is the parasitic capacitance at the output of OTA2. Considering the condition $2GB < \omega_{p2}$ is typically used to ensure sufficient phase margin to avoid oscillation, the following expression for C_c must be meet:

Fig. 3. Simulated impedance of the multiplier using different values of R resulting in multiplication factors of $k = 16, 160, 1.6k$ and $16k$ split into magnitude and phase.

Fig. 4. Simulation results of a Montecarlo test split into magnitude and phase showing that the equivalent impedance remains unchanged when fabrication variations are considered.

$$C_c > C_{o2} \left[\frac{2g_{m1}r_{o1}g_{m2}r_{o2}^2}{R} \right]$$

With this addition, the numerator of Z_o takes the form:

$$s^2[CC_cr_{o1}R] + s[C(r_{o1} + R) - C_cr_{o1}] - [1 + g_{m1}r_{o1}]$$

From which the new zeros can be calculated; the pole at low frequency remains unchanged.

4 Simulation and experimental results

The floating architecture in Fig. 1e was simulated using Spectre, and fabricated in $0.5\mu\text{m}$ C5N technology through MOSIS. The nominal threshold voltages are $V_{\text{THN}} = 0.7\text{ V}$ and $V_{\text{THP}} = 0.9\text{ V}$, and the transistor sizes are $30/1.2$ and $90/1.2\mu\text{m}/\mu\text{m}$ for the NMOS and PMOS respectively. The circuit was tested with a supply voltage of $V_{\text{DD}} - V_{\text{SS}} = 2.2\text{ V}$ and a biasing current of $50\mu\text{A}$, which results in a drain-source saturation voltage of $V_{\text{DSsat}} \approx 0.17\text{ V}$. The values of the capacitors and resistors are $C = 10\text{ pF}$, $C_c = 3\text{ pF}$, $R = 5\text{ M}\Omega$ and $R_k = 5\text{ k}\Omega$ and it has a gain of the FFVF of $A_{\text{vf}} = 0.83$, which gives a scaling factor of $k = 16.6\text{ k}$. With these values circuit simulation shows an equivalent capacitance of $C_{\text{eq}} = 16.6\text{ nF}$, $\omega_p = 60\text{ Hz}$, $\omega_z = 43\text{ kHz}$, $\text{PLR} = 158\text{ k}\Omega$, and $\text{ESR} = 223\Omega$.

Fig. 3 shows the simulated equivalent impedance of the multiplier split into magnitude and phase for $R = 50\text{ k}$, 500 k , 5 M and $50\text{ M}\Omega$, which give scaling factors of $k = 16$, 166 , 1.6 k and 16 k , respectively. Fig. 4 shows the simulation results of the Montecarlo test for $R = 50\text{ M}\Omega$; observe that the corners and frequency limits are affected by variations due to fabrication; however, the resulting impedance within the operational frequency range remains unchanged, thus offering high accuracy. The floating version of the multiplier (Fig. 1e) was fabricated and tested in an RLC notch filter considering the values $C_{\text{eq}} = 16.6\text{ nF}$, an inductor $L = 100\text{ mH}$, and a resistor $R_L = 1\text{ k}$, 10 k , and $100\text{ k}\Omega$. The microphotograph of the circuit is shown in Fig. 5, and the experimental plots are depicted in Fig. 6.

Table I shows a comparison of measured parameters between previously reported multipliers and the proposed circuit.

Fig. 5. Microphotograph of the fabricated circuit ($318\ \mu\text{m} \times 232\ \mu\text{m}$).

Fig. 6. Experimental results showing the operation of the multiplier implemented in an RLC notch filter for $R_L = 1\ \text{k}\Omega$, $10\ \text{k}\Omega$, and $100\ \text{k}\Omega$.

Table I. Compared results between conventional and proposed capacitance multipliers.

Parameter	[4] 2009	[3] 2012	[6] 2013	[1] 2015	[2] 2015	This work
CMOS Technology [μm]	OTAs ¹	0.5	0.5	0.5	0.18	0.5
Base capacitance [pF]	1000	18	10	25	10	10
Multiplication factor	22	10.1	10 k	28	50	16.6 k
C_{eq} [nF]	22	0.18	10	0.7	0.5	16.6
Supply voltage [V]	5	2.7	3	2.2	1.8	2.2
Power consumption [mW]	28.7	1.75	1.81	1.32	5.72	1.1/2.2 ²
Effective BW [MHz]	-	-	1.3	0.5	0.011	43 k
ESR [Ω]	-	-	218	392	-	223
PLR [$M\Omega$]	1.5	-	-	1.28	-	0.158
Silicon area [mm^2]	-	0.07	0.042	0.07	0.002	0.073

¹Commercial IC CA3280

²Grounded and floating implementations respectively

5 Conclusion

A capacitance multiplier that depicts high accuracy with reduced power consumption and silicon area was discussed. Resistive ratios by means of appropriate layout techniques yield to high accuracy and large multiplication factors. This is achieved by scaling the voltage swing of the current-providing amplifier, which reduces the static power consumption considerably compared to the conventional current-mode technique. Experimental results show the effective application of the proposed circuit in a practical implementation.