Low power hybrid PG_Filter-AGC analog baseband for wireless receivers

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Abstract: A low power hybrid PG_Filter-AGC analog baseband is presented, including a programmable filter (*PG_filter*) and an auto gain control core (*AGC_core*). It adopts the digital-plus-analog mixed gain control methodology, resulting in an effective power reduction and a decibel gain error improvement. To further reduce the power of the *AGC_core*, a low power Variable Gain Amplifier (VGA) adopting sub-threshold design methodology is presented. Furthermore, a self-adaptive threshold voltage compensation (SATC) scheme is proposed to guarantee the good anti-process variation performance for sub-threshold design methodology. The hybrid analog baseband has been fabricated under SMIC 0.18 μm CMOS process, with a die size of 0.45 mm², where the *AGC_core* occupies an area of 0.28 mm². The test results demonstrate a total power of 4.1 mW, where the *AGC_core* consumes a power of 0.39 mW. A consecutive gain dynamic range of 80 dB, with a decibel gain error small than ± 0.39 dB, is achieved and the cutoff frequency ranges from 0.5 MHz~30 MHz.

Keywords: low power, analog baseband, sub-threshold, hybrid, AGC

Classification: Integrated circuits

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1 Introduction

The analog baseband composed of intermediate frequency (IF) filter and Auto Gain Control (AGC) circuit is an indispensable circuit block for wireless receiver. The AGC plays an important role in stabilizing the output power of the receiver and relaxes the required dynamic range of cascaded analog to digital converter (ADC). The IF filter selects desired signals from interferences and anti-aliases unwanted noise and blockers. Both of these two circuits are crucial for excluding unwanted effects, such as the interferences, aliased noise, and gain variation [1].

Power consumption is increasingly becoming the dominant factors and inevitable urgent requirements for wireless receivers, especially when taking into account of the explosive growth of mobile, portable applications [2, 3]. This is also quite an issue for the analog baseband. However, most studies, which tend to require huge power, do not pay sufficient attention to these issues [3, 4].

In this work, a low power hybrid PG-filter-AGC analog baseband is proposed. By adopting a hybrid architecture, a digital-plus-analog mixed gain control methodology is achieved. Then, the required gain dynamic range of *AGC_core* is relaxed. As a result, a less gain of the *AGC_core* is required, and the power of the analog baseband is reduced from the system level design. Moreover, a less gain dynamic range also results in an improved decibel gain error of *AGC_core*.

For the *AGC_core*, the necessary decibel linear gain control characteristic of VGA is crucial for stabilizing the settling time of the AGC loop. For full-CMOS implementation of VGA, typical approaches include the digital or analog design strategy. The digital solutions usually adopt a switchable resistor network [5], while the analog solutions include the Taylor series approximation [6] or the pseudo-exponential approximation [7]. However, these solutions suffer from high-power and large decibel gain error, especially when a large gain dynamic range is required. These defects greatly restrict their application prospect when facing the urgent low power requirement.

With the progress of the semiconductor technology and design strategy, the sub-threshold design methodology, which demonstrates a well exponential I-V curvature, has been verified as a realistic low-power solution. Lee [8] has verified the reliability of the sub-threshold low noise amplifier (LNA) and the feasibility of the sub-threshold voltage controlled oscillator (VCO) [9]. A sub-threshold voltage reference is proposed by Du [10] with satisfactory performance. The sub-threshold design methodology also provides a new low power solution for VGA.

In this work, a low power VGA adopting sub-threshold design methodology is proposed. Furthermore, a self-adaptive threshold compensation (SATC) methodology is introduced to guarantee a good anti-process variation performance for the sub-threshold design methodology.

The hybrid analog baseband has been fabricated in SMIC 0.18 μm CMOS process. Test results demonstrate a dynamic gain range of 80 dB with a decibel gain error small than ± 0.39 dB, while the cut-off frequency ranges from 0.5 MHz~30 MHz. The total power of the hybrid analog baseband is 4.1 mW, where the *AGC_core* consumes a power of 0.39 mW.

2 System architecture

The proposed analog baseband shown in Fig. 1 adopts a hybrid architecture, where the *PG_filter*, whose gain is digitally programmable, is subsumed into the AGC gain control loop and acts as the gain stage of the VGA. As a result, by cascading the *PG_filter* and a VGA with an analog consecutive controllable gain, a digital-plus-analog mixed gain control strategy is achieved. Then, even with a small gain dynamic range of VGA, a large gain dynamic range of the analog baseband is

Fig. 1. Architecture of the proposed hybrid analog baseband

achieved, and the decibel gain error is only determined by the VGA, as shown in Fig. 2. In this work, the gain dynamic range of the VGA is 23 dB (including a 3 dB redundant gain for gain variation suppression). Combined with the *PG_filter*, the gain step of which is set to be 20 dB, a gain dynamic range of 80 dB of the analog baseband is achieved.

With the above architecture design methodology, a less gain dynamic range of VGA is required, which means less gain stages of VGA. Consequently, the power and hardware cost of the VGA is greatly reduced. Moreover, a smaller dynamic gain range of the VGA also means a smaller decibel gain error. With the hybrid digital-plus-analog mixed gain control strategy, the reduction of the gain dynamic range of VGA also helps reducing the decibel gain error of the analog baseband, as the decibel gain error is determined by the VGA, which is also shown in Fig. 2.

Fig. 2. Scheme of the digital-plus-analog mixed gain control strategy

3 Detailed circuit design of hybrid analog baseband

A. The VGA adopting sub-threshold design methodology

a) Architecture design

Fig. 3(a) shows the configuration of the proposed VGA. The sub-threshold exponential current generator (*Iexp-gen*) and the SATC block form the sub-threshold decibel gain control circuit to realize decibel gain for VGA. There are two *gain stages* for the VGA and each *gain stage* is comprised of two sub-amplifiers. The gain characteristic of the sub-amplifier is shown in the upper-left side of Fig. 3(a). When the exponential I-V function between V_{cg} and I_{exp} holds, the gain of the VGA demonstrates a good decibel gain characteristic. Then, how to achieve the exponential I-V function between V_{cg} and I_{exp} is crucial.

M_{exp} , the core transistor of *Iexp-gen* is biased in the sub-threshold region. According to the well-established exponential I-V curvature of sub-threshold MOS transistor [8, 9, 10], the function between V_{cg} and I_{exp} can be expressed as:

$$I_{exp} = I_{s0} S_{M_{exp}} \exp\left(\frac{V_{cg} - V_{th} - V_{off}}{nV_T}\right) \left(1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right) \quad (1)$$

$$I_{s0} = \mu_0 \sqrt{\frac{q\epsilon_{si}N_{ch}}{2\Phi_s V_T}} \quad (2)$$

where: S and V_{th} is the aspect ratio and threshold voltage, V_{ds} is the drain and source voltage difference. $V_T = kT/q$ (26 mV@27°C). n is defined as the differ-

Fig. 3. Full circuit of the proposed VGA

ential of the gate voltage V_G to the cut-off voltage V_p , which ranges from 1 to 2. V_{off} is the gate-source voltage tested when $I_{ds} = 0$, and for the process adopted in this work, $V_{off} = 130$ mV. μ_0 , ϵ_{si} , Φ_s and N_{ch} are parameters defined by process.

When $V_{ds} > 4V_T$, the last term in Eq. (1) can be neglected. $I_{s0}S_{Mexp}$ is a constant when design parameters are set, and supposed it equal to λ , then:

$$I_{exp} = \lambda \exp\left(\frac{V_{cg} - V_{th} - V_{off}}{nV_T}\right) \quad (3)$$

Then, the exponential I-V function between V_{cg} and I_{exp} holds, and the decibel gain tuning characteristic of the VGA is guaranteed.

The exponential I-V curvature of sub-threshold MOS transistor is crucial for the sub-threshold design methodology. However, as shown in Eq. (3), I_{exp} shows a direct correlation with V_{th} . The variation of V_{th} may be bigger than 100 mV or even larger. Thus, two main problems in the sub-threshold design methodology is presented: 1) MOS transistor should be biased in sub-threshold region reliably to guarantee the exponential I-V curvature; 2) the process variation of V_{th} is of great concern, which may cause a huge variation of I_{exp} or even drive MOS transistor out of sub-threshold region. Both problems can collapse the performance and even the function of the exponential I-V curvature between V_{cg} and I_{exp} . However, to the authors' knowledge, few studies reports solutions to these problems.

To address the questions for sub-threshold design methodology, a SATC block shown in Fig. 3(a) is introduced. With the help of the SATC block, which will be proved in the following text, M_{exp} is biased in sub-threshold region reliably. Moreover, the process variation of V_{th} is simultaneously cancelled, which guarantees a stable exponential I-V curvature between V_{cg} and I_{exp} . Finally, a stable decibel gain of the VGA even under huge process variation is guaranteed.

b) SATC scheme and circuit design

The schematic of the *V-I converter* is shown in Fig. 3(b). Then, the voltage difference across the gate and source of M_{exp} , V_{cg} , can be deduced as:

$$V_{cg} = V_{gs, Mexp} = \frac{M}{N} \frac{R_0}{R_1} V_{ctrl} + V_{dth} \quad (4)$$

where, V_{dth} generated by the *Vth-detector* is a crucial parameter for SATC scheme, as proved in the following formulas.

The schematic of the *Vth-detector* is shown in Fig. 3(c). Transistor m1~m4 are all biased in the sub-threshold region, and transistor m3 works as a pseudo-diode. Combined with amplifier A_0 , three feedback loops as shown in Fig. 3(c) are achieved, the total gain of which forces $V_a \approx V_b$, and this is the base for the following deduction. It should be note that, the introduction of the pseudo-diode helps to improve the total loop gain of the *Vth-detector*. This helps V_a and V_b equal to each other more accurately, as proved in **Appendix A**.

Then, the detected threshold voltage is:

$$V_{dth} = V_{th} + V_{off} + nV_T \ln \left[\frac{nV_T S_1}{R_2 S_2 S_3 I_{s0}} \ln \left(\frac{S_1}{S_2} \frac{S_4}{S_3} \right) \right] \quad (5)$$

When V_{cg} is applied on *Mexp*, I_{exp} can then be expressed as:

$$I_{exp} = \lambda \exp \left\{ \ln \left[\frac{nV_T S_1}{R_2 S_2 S_3 I_{s0}} \ln \left(\frac{S_1}{S_2} \frac{S_4}{S_3} \right) \right] + \frac{M}{N} \frac{R_0}{R_1 nV_T} V_{ctrl} \right\} \quad (6)$$

The first term in the exponential function and the coefficient of V_{ctrl} are denoted as α and β respectively, then:

$$I_{exp} = \lambda \exp(\alpha + \beta V_{ctrl}) \quad (7)$$

As long as the design parameters are set, α , β and λ are all constants. Then, Eq. (7) shows that I_{exp} is only determined by control voltage V_{ctrl} , while V_{th} is cancelled by V_{dth} . Moreover, when all design parameters are reasonably set to make:

$$\frac{M}{N} \frac{R_0}{R_1} V_{ctrl} + \alpha nV_T + V_{off} < 0 \quad (8)$$

then, $V_{cg} = V_{gs, Mexp} < V_{th}$ will always holds, *Mexp* is always biased in sub-threshold region reliably, even with a large process variation. Moreover, the variation of I_{exp} due to V_{th} drift is also compensated, which can be seen from Eq. (3) and (7).

Based on the above analysis, the problems of sub-threshold design methodology mentioned above are successfully solved, which guarantees good performance and robustness of the proposed sub-threshold decibel gain control circuit.

c) Gain stage design

To realize the *gain stage* with a gain characteristic as shown in upper-left side of Fig. 3(a), the most simple and direct way is adopting two cascaded sub-amplifiers with resistive load, as shown in Fig. 4. However, under the bias of a changing exponential current for gain tuning, the output quiescent output voltage of each sub-amplifier is: V_1 (or V_{op}) = RI_{exp} . As a result, the gain controlled by tuning I_{exp} will result in a huge deviation of the quiescent operation point of the sub-amplifier. This is of great danger, which may drive the sub-amplifier into linear or off region. As a result, the allowable operating range is restricted, and the gain dynamic range of the VGA is also narrowed, as shown on the right side of Fig. 4.

To stabilize the quiescent operation point of the sub-amplifier, a current network loaded sub-amplifier is proposed, as shown in Fig. 3(d). It is composed of a diode connected MOS transistor and a current source biased by I_{exp} . Then, the output quiescent operation point of each sub-amplifier can be re-written as:

$$V_1(or V_{op}) = \sqrt{\frac{2I_{dc}}{\mu_n C_{ox} S_9}} + V_{th} \quad (9)$$

Thus, the output quiescent operation point of each sub-amplifier remains stable, even under a large variation of the exponential current I_{exp} for gain tuning.

Fig. 4. Schematic of sub-amplifier of VGA and the narrowed operating range

According to Fig. 3(d), with reasonable parameters setting, the gain of each *gain stage* can be derived as:

$$G_{exp} = A_{sub-amplifier}^2 = \left(\frac{g_{m7}}{g_{m9}} \right)^2 = \frac{S_{m7}}{S_{m9}} \left[1 + \frac{\lambda}{I_{dc}} \exp(\alpha + \beta V_{ctrl}) \right] \quad (10)$$

With proper design parameters settings, the constant “1” in the square brackets can be neglected (this approximation may introduce some decibel gain error. Nevertheless, the hybrid architecture of the analog baseband helps to reduce the gain tuning rang of the VGA, and decibel gain error is also reduced to a negligible level as mentioned above), then:

$$\ln(G_{exp}) = \eta + \beta V_{ctrl}, \quad \eta = \alpha + \ln\left(\frac{S_{m7}}{S_{m9}} \frac{\lambda}{I_{dc}}\right) \quad (11)$$

Eq. (11) indicates good decibel gain of the VGA. Moreover, as the V_{th} variation of I_{exp} has been compensated by the proposed SATC scheme, the gain of the *gain stage* of VGA is also only determined by the control voltage V_{ctrl} . Finally, a stable gain of VGA is achieved despite the process variation.

B. Ctrl-loop circuit design

The loop control circuit *Ctrl_loop* is shown in Fig. 5, where the *Clamp circuit* is used to set the highest voltage level of V_{ctrl} to guarantee Eq. (8) always holds. The *Peak_detector* senses the highest voltage level of the output of the analog baseband, while the target output amplitude is set by V_{amp} (the input of the *Error amplifier*).

Fig. 5. Architecture of the *Ctrl_loop*

The *Comparator logic* generates 4 bits digital control code *G_prg*, and it is then send into the *PG_filter* to decide the digital gain of the *PG_filter*.

Moreover, the *Error amplifier*, *Clamp circuit* and *Comparator logic* are all biased in the sub-threshold region to save power without sacrificing performance, while the *Peak detector* is biased in the saturation region for a higher work speed.

Fig. 6. Circuit design for *PG_filter*

C. Citcuit desing of *PG_filter*

For *PG_filter*, the Sallen-Key Biquade filter synthesizing method is discarded for its sensitivity to the process variation and the parasitic effect. In this study, the Tow-Thomas Biquade filter synthesizing method is adopted for its relatively high stability and low sensitivity to the parasitic effect and the process variation.

Fig. 6 shows the schematic of the 4th-order butterrworth (which is chosen for its relax requirements on core operational amplifier) low pass *PG_filter*. It has two cascade 2nd-order Tow-Thomas Biquades, with the transfer function expressed as:

$$H(s) = \frac{1}{R_1 R_2 C_1 C_2} \frac{1}{s^2 + \frac{s}{R_3 C_1} + \frac{1}{R_2 R_4 C_1 C_2}} \quad (12)$$

Then, the detail parameters of the Tow-Thomas Biquade including pass-band gain, 3-dB cut-off frequency and *Q* factor are shown as follows:

$$A_0 = \frac{R_4}{R_1}, \quad f_c = \frac{1}{2\pi\sqrt{R_2 R_4 C_1 C_2}}, \quad Q = \frac{R_3}{\sqrt{R_2 R_4}} \sqrt{\frac{C_1}{C_2}} \quad (13)$$

The methodology of setting the design parameters is of great importance to realize an independent cut-off frequency programming and digital gain control, without changing the Q factor. Then, the following strategy is adopted: tunable resistor R_1 under the control of G_prg is responsible for digital gain control. Adjustment of the product of C_1 and C_2 under the control of BW_prg is responsible for the cut-off frequency manipulating, while C_1/C_2 remains to be a constant and R_2 , R_3 and R_4 remain unchangeable to keep a stable Q factor.

Fig. 7. Die photo of (a) the independent AGC_core ; (b) the full hybrid analog baseband

4 Measurement results

The analog baseband was fabricated under SMIC 0.18 μm CMOS technology. The VGA determines the performance of the analog baseband. Thus, an independent AGC_core is taped out and a performance test is setup individually. The photo is shown in Fig. 7(a) with an area of 0.28 mm^2 , including the $Ctrl_loop$ but without test pads.

Two test modes for AGC_Core are adopted, including an open loop test and a closed loop test: 1) the open loop test is dedicated for the performance of VGA. It is realized by forcing a programmable voltage source on V_{ctrl} . The performance of the proposed VGA is summarized in Table I, which shows much lower power compared with previous works. The test results in Fig. 8 show that the dynamic gain range is 23 dB while the decibel gain error is less than ± 0.39 dB. The test results demonstrate the correct function and good performance of the proposed

Fig. 8. Gain and dB error of VGA with respect to V_{ctrl}

VGA; 2) A transient closed loop test is then carried out. The test result is shown in Fig. 9, which demonstrate the good performance of the proposed *AGC_core*.

Table I. Performance of the sub-threshold VGA

Parameters	[5]	[6]	[11]	[12]	This Work
Power source/V	1.8	1.8	1.8	2.5	1.8
Number of gain stages	3	1	3	4	2
Gain range/dB	95	48	60	80	23
dB-error/dB	NA	NA	NA	± 3	± 0.39
Bandwidth/MHz	32	3	16	30~210	30
Power/mw	6.5	0.55	3.6	11	0.39*

*The power listed here is in fact the power of *AGC_core* including the power of the *Ctrl_loop*.

Fig. 9. Closed loop transient test results of the *AGC_core*

Fig. 7(b) shows the photo of the hybrid analog baseband, occupying a die area of 0.45 mm^2 without test pads. The performance summary is shown in Table II. Due to the hybrid architecture, the dynamic gain of the hybrid analog baseband reaches 80 dB, while the *AGC_core* only provides a dynamic range of 23 dB. The total power is 4.1 mW. As compared to former reports, the proposed analog baseband is power and cost efficient.

Table II. Performance of the hybrid analog baseband

Parameters		[3]	[13]	This work
Gain control type		Digital	Digital	Digital-plus-analog mixed, Consecutively
Power source/V		1.2	1.2	1.8
Maximum Power/mW	PG_filter	—	21.6	3.71
	AGC_core	—	13.5	0.39
	Total	9.6	35.1	4.1
Gain dynamic range/dB		72	39	80
Cut-off frequency/MHz		0.2~20	0.35~23.5	0.5~30
Technology		65 nm	0.13 μm	0.18 μm
Circuit Area/ mm^2		0.8	1.56	0.45 (<i>AGC_core</i> : 0.28, including the <i>Ctrl_loop</i>)

The cut-off frequency of the analog baseband is shown in Fig. 10(a), which demonstrates a programmable bandwidth ranging from 0.5 MHz to 30 MHz. The overall gain characteristic of the full analog baseband with the respect of input

frequency is shown in Fig. 10(b). Fig. 11 gives the measured closed loop gain and dB error of the full hybrid analog baseband circuits with respect to V_{ctrl} , which shows the monotonically increasing of the gain with respect to the reduction of the input signal strength. Moreover, the dB error test result (which is smaller than ± 0.39 dB) also demonstrates that, the same as depicted in Fig. 2, the hybrid digital-plus-analog mixed gain control strategy of this work helps to improve the decibel gain error of the full hybrid analog baseband.

Fig. 10. (a) Measured cut-off frequency response of the full analog baseband; (b) Measured gain response of the full analog baseband

Fig. 11. Gain and dB error of the full hybrid analog baseband circuits with respect to V_{ctrl}

5 Conclusion

A low power hybrid analog baseband is proposed in this study. By adopting a digital-plus-analog mixed gain control methodology, the gain dynamic range of the VGA is relaxed. Thus, the power of the analog baseband is optimized at the system level. Moreover, with a reduced gain tuning range of the VGA, the decibel gain error of the full analog baseband is also improved. For the *AGC_core*, the sub-threshold design methodology is adopted for power reduction, while the process variation of sub-threshold design methodology is compensated by a SATC scheme. Moreover, a pseudo diode helping in enhancing the loop gain is introduced to improve the performance of the SATC scheme, while a current network loaded amplifier for the *gain stage* of VGA is proposed to stable the quiescent operating point. The test results demonstrate a total power dissipation of 4.1 mW, while the *AGC_core* dissipates 0.39 mW. The total gain dynamic range of the full analog baseband is 80 dB with a ± 0.39 dB decibel gain error.

Fig. 12. Schematic of the prototype of *Vth-detector*

Appendix A: Improvement of the loop gain of *Vth-detector*

The prototype of *Vth-detector* is a sub-threshold I_{PTAT} current generator illustrated in Fig. 12 [14]. The calculation foundation for this circuit is the assumption of $V_a = V_b$. How V_a and V_b approach to each other is crucial. For the traditional design as shown in Fig. 12, this assumption is guaranteed by the positive feedback loop 1 and the negative feedback loop 2. Thus, the total loop gain is:

$$LG = g_{m2} \left[r_{o2} \parallel \left(R_1 + \frac{1}{g_{m4}} \right) \right] A_0 - g_{m1} \left(r_{o1} \parallel \frac{1}{g_{m3}} \right) A_0 \quad (14)$$

where: r_o is the small signal resistance of MOS transistor, and $g_{m3} = g_{m4}$, $g_{m1} = g_{m2}$.

When $r_o \gg 1/g_m$ and $r_o \gg R_1$, the loop gain falls into the range of $g_m r_o A_0$.

V_a accurately equal to V_b is crucial to the precision of the detection of V_{th} and for the performance of the SATC scheme. Thus, a higher loop gain is essential.

To improve the loop gain, a pseudo diode connected transistor similar to our previous study is introduced, as shown in the grey block in Fig. 3(c). As a result, a new additional negative feedback path marked as loop 3 in Fig. 3(c) is introduced. Then, the total loop gain can then be re-expressed as:

$$LG = g_{m2} \left[r_{o2} \parallel \left(R_2 + \frac{1}{g_{m4}} \right) \right] A_0 - g_{m2} \left[r_{o2} \parallel \left(R_2 + \frac{1}{g_{m4}} \right) \right] g_{m3} (r_{o1} \parallel r_{o3}) A_0 - g_{m1} (r_{o1} \parallel r_{o3}) A_0 \quad (15)$$

Assume that r_o is much larger than $1/g_m$, and R_2 , and $g_{m3} = g_{m4}$, $g_{m1} = g_{m2}$, then the loop gain of the proposed *Vth-detector* can be simplified as:

$$LG = -g_{m1} (r_{o1} \parallel r_{o3}) A_0 \left[r_{o2} \parallel \left(R_2 + \frac{1}{g_{m4}} \right) g_{m3} + 1 \right] \cong -g_{m1} g_{m3} (r_{o1} \parallel r_{o3}) r_{o2} A_0 \quad (16)$$

It can be concluded that the loop gain when introducing the pseudo diode falls into the range of $(g_m r_o)^2 A_0$. Thus, the total loop gain is enhanced by $g_m r_o$ times. This will accurately force $V_a = V_b$, which also guarantees the precision of the *Vth-detector*, and finally, the performance of the SATC is improved.

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