A 12.8 nA and 7.2 ppm/°C CMOS voltage reference without amplifier

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Abstract: Based on the negative feedback technique, an ultra-low-power CMOS voltage reference without amplifier is proposed using a 0.18 µm CMOS technology. The proposed voltage reference achieves a temperature coefficient (TC) of 7.2 ppm/°C when the temperature ranges from −20 °C to 80 °C, only consuming 12.8-nA current at room temperature. Besides, the minimum supply voltage is 0.75 V and line sensitivity (LS) is 0.24 mV/V when supply voltage ranges from 0.75 V to 3.5 V. The power supply rejection ratio (PSRR) is only −79 dB at 100 Hz, −56 dB at 1 MHz, respectively.

Keywords: voltage reference, CMOS, ultra-low power, PSRR

Classification: Integrated circuits

References


1 Introduction

As an important part of analog and mixed-signal integrated circuits, voltage reference provides a stable and constant DC voltage, which means the voltage is independent of supply voltage, temperature and manufacturing process. Nowadays, since portable devices such as smartphones, tablets and wearable devices are widely used, where battery replacement is troublesome, low power becomes the crucial design point for the chips, which embraces the low current and low supply voltage.

Traditional band-gap voltage references use parasitic vertical BJTs and resistances to obtain a zero temperature coefficient (TC) [1]. The area would be large and the resistances mismatch worsens the accuracy. Besides, they typically provide a 1.2-V voltage and require high supply voltage, therefore CMOS voltage reference is introduced [2, 3, 4]. [5] uses weighted gate-source voltage difference to achieve temperature-compensated voltage reference by two types of transistors with different threshold voltages. The total current is 40 nA. [6] also uses a high threshold voltage (HVT) MOSFET, and current is only 7 nA, but the TC is as high as 142 ppm/°C. [7, 8] and [9] obtain temperature compensation by the body effect and the two source coupled pairs, respectively, but the supply voltage and the current are still not low enough, which are more than 0.85 V for [7] and 214 nA for [9], respectively.

To improve the performances of low current, low supply voltage and low TC, a CMOS voltage reference by taking advantage of body bias and negative feedback techniques is proposed in this paper. Benefiting from the negative feedback effect, the amplifier is omitted to reduce current and improve the anti-noise ability of the circuit. Besides, the body effect is considered to improve the accuracy of temperature compensation. With abovementioned measurements, the proposed circuit operates with a 0.75-V supply voltage, consumes current as small as 12.8 nA and obtains a TC as low as 7.2 ppm/°C.

This paper is organised as follows: Section 2 and Section 3 describe the circuit implementation and the negative feedback technique in detail, respectively; in Section 4, the simulation results are shown and analysed; finally a conclusion is drawn in Section 5.
2 Circuit implementation

Fig. 1 shows the schematic of the proposed voltage reference. It consists of a start-up circuit, a current source and a negative feedback circuit. The start-up circuit is designed to achieve the normal operation condition. M3 is a HVT MOSFET with $V_{THH}$, while all other transistors in the proposed voltage reference are the MOSFETs with standard threshold voltage (SVT) $V_{TH}$. In this circuit, PM1 and PM2, operating in the subthreshold region with the same aspect ratio, compose a current mirror to impose equal currents in the two branches of the circuit. Together with current mirror, M1~M4 form the current source. The gate voltages of M1 and M2 are equal and we can obtain:

$$V_{GS1} + V_{GS2} = V_{GS3}$$

(1)

Since M3 has a larger threshold voltage $V_{THH}$ than M1, M3 and M1 are biased with the same current with different gate-source voltages. The I-V characteristic of a transistor, operating in the subthreshold region, can be approximated by:

$$I_{DS} = \mu C_{ox} K (\eta - 1) V_T^2 \exp \left( \frac{V_{GS} - V_{TH}}{\eta V_T} \right) \times \left[ 1 - \exp \left( \frac{-V_{DS}}{V_T} \right) \right]$$

(2)

where $\mu$ is the carrier mobility, $C_{ox}$ is the gate-oxide capacitance, $\eta$ is the sub-threshold slope factor and $K = W/L$ is the aspect ratio. Besides, $V_T$ is the thermal voltage and $V_T = k_B T/q$, where $k_B$ is the Boltzmann constant, $T$ is the absolute temperature and $q$ is the elementary charge. In this paper, since $V_{DS} \geq 4V_T$, the channel length modulation is neglected. The gate-source voltage can be derived as:

$$V_{GS} = V_{TH} + \eta V_T \ln \left( \frac{I_{DS}}{\mu C_{ox} K (\eta - 1) V_T^2} \right)$$

(3)

Using Eq. (3) to extract the gate-source voltages of M1-M3, Eq. (1) can be given as:
\[ V_{TH}^{*} + \eta V_T \ln \left( \frac{m I}{\mu_n C_{ox} K_1 (\eta - 1) V_T^2} \right) + V_{TH} + \eta V_T \ln \left( \frac{m I}{\mu_n C_{ox} K_2 (\eta - 1) V_T^2} \right) \]

\[ = V_{HTH} + \eta V_T \ln \left( \frac{I}{\mu_n^* C_{ox}^* K_3 (\eta - 1) V_T^2} \right) \]

(4)

where \( V_{TH}^{*} \) is the threshold voltage with body effect. Besides, \( \mu_n \) and \( C_{ox} \) are the carrier mobility and the gate-oxide capacitance of the HVT MOSFET, respectively. \( \mu_n^* \) is almost equal to \( \mu_n \) of SVT MOSFET, while \( C_{ox}^* \approx 2.2 C_{ox} \). Considering that the source body voltage of M1, namely \( V_{SB1} \) is small, \( V_{TH} \) can be approximated by \[7, 10]\:

\[ V_{TH} = V_{TH} + (\eta - 1) V_{SB1} = V_{TH} + (\eta - 1) V_{GS2} \]

(5)

We can derive the expression of \( I \) as:

\[ I = \frac{1}{n} \mu_n C_{ox} K_2 (\eta - 1) V_T^2 \left( \frac{K_1}{2.2mK_3} \right)^{\frac{1}{\eta}} \exp \frac{V_{HTH} - (1 + \eta) V_{TH}}{\eta V_T} \]

(6)

The negative feedback circuit, used to keep the current mirror with good matching, also generates the reference voltage. As shown in Fig. 1, M6 is diode connected and biased by a current mirroring \( I \) in the ratio of \( \beta (= K_{P3}/K_{P1}) \). Substituting Eq. (6) into Eq. (3), \( V_{ref} \) can be expressed as:

\[ V_{ref} = \frac{1}{\eta} (V_{HTH} - V_{TH}) + V_T \left( \frac{\eta \beta K_2}{n K_6} + \ln \frac{K_1}{2.2mK_3} \right) \]

(7)

It is obvious that \( V_{ref} \) is a linear combination of \( V_{TH} \) with negative TC and \( V_T \) with positive TC. Setting \( \partial V_{ref}/\partial T = 0 \), an output reference voltage independent of temperature can be obtained in the case of:

\[ \frac{1}{\eta} (\kappa - \kappa_H) + \frac{k_B}{q} \left( \frac{\eta \beta K_2}{n K_6} + \ln \frac{K_1}{2.2mK_3} \right) = 0 \]

(8)

where \( \kappa \) and \( \kappa_H \) are the TC of \( V_{TH} \) and \( V_{HTH} \), respectively.

3 Negative feedback

When supply voltage varies, the bias current varies because of the channel length modulation and it causes the variation of the reference voltage. In order to reduce the channel length modulation effect and make sure that the currents in two branches match better, a negative feedback loop formed by M4, M5, M6 and PM3 is proposed instead of the traditional differential-input amplifier.

Assuming there is an incremental voltage variation at node \( b \) with the supply voltage variation, the voltage of node \( c \) would fall, and then the voltage of node \( a \) would rise. Since the gain of the negative feedback loop formed by M1, M3, M5 and PM3 is greater than that of the positive feedback loop formed by M5, PM3 and PM2, the voltage of node \( b \) would fall at last, and vice versa. It is the existence of negative feedback loop that guarantees the constancy of the current against the supply voltage variation. Therefore, the mismatch introduced by channel length modulation can be reduced significantly, and long channels for transistors are not as necessary as in the conventional structures, which makes a contribution to diminishing the chip area. What’s more, the negative feedback circuit also plays the role of amplifier, thus reducing the chip area and quiescent current.
Fig. 2 shows the small signal model of the PSRR in low frequency, which can be expressed by:

\[
\text{PSRR} \approx 20 \log \frac{g_{mp1} - g_{mp1}}{g_{m3}} - \frac{g_{mp1}}{g_{m2}} - \frac{g_{mp2}}{g_{m3}} \left( \frac{1}{g_{m2}} - \frac{1}{g_{m1}} \right)
\]

where \( g_{oi} \) and \( g_{mi} \) represent the output conductance and transconductance of \( M_i \) (\( i = 1, 2, p1, p2 \ldots \)), respectively. As shown in the Eq. (9), the sensitivity to the supply noise decreases by increasing the ratio of \( g_{m6}/g_{mp3} \) benefited from the negative feedback.

**4 Simulation results**

To estimate the performances of the proposed voltage reference, a series of simulations have been implemented using 0.18 µm CMOS technology. As shown in Fig. 3(a), when \( V_{DD} = 0.75 \) V, which is the minimum supply voltage, the TC is 8.2 ppm/°C. When \( V_{DD} \) is 3.5 V, the maximum supply voltage, TC increases to 9.7 ppm/°C. The best TC is 7.2 ppm/°C, obtained when \( V_{DD} \) is 1.8 V. The quiescent current is 12.8 nA at room temperature and varies from 5.3 nA to 25.7 nA when the temperature changes from −20° to 80°, as shown in Fig. 3(b). It can be concluded that the quiescent current is almost independent of \( V_{DD} \).

In order to ensure correct function of the circuit against process variation, Monte Carlo analyses for 450 samples are carried out, assuming that all relative parameters follow a Gaussian distribution under the condition of the typical process corner and room temperature. The results are depicted in Fig. 3(c) and Fig. 3(d). There are 172 samples whose TC is lower than 10 ppm/°C while only 6 samples higher than 60 ppm/°C. The mean value and the standard deviation of TC are 16.7 and 12 ppm/°C, respectively, and the coefficient of variation \( \sigma/\mu \) is 71.9%. The mean value of the reference voltage is 319 mV and the standard deviation \( \sigma \) is 4 mV, the coefficient of variation \( \sigma/\mu \) is 1.27%. Fig. 3(e) shows that, the output voltage of the reference has a difference of 0.65 mV with the supply voltage ranging from 0.75 V to 3.5 V, which implies LS is 0.24 mV/V, namely 752 ppm/V.

Fig. 2. Small-signal equivalent model of PSRR.
shows that PSRR is $-79$ dB at 100 Hz, $-60$ dB at 1 KHz and $-57$ dB at 1 MHz at room temperature with supply voltage of 1.8 V and without any filtering capacitor.

Table I lists the main performances comparison with other CMOS references. As shown in Table I, better LS with HVT MOSFET than [11], better TC than [7] and [11], smaller supply voltage and current than [7] and [9] and best PSRR benefited from the negative feedback than all other designs are obtained.

<table>
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<th>[7]</th>
<th>[9]</th>
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<td>Supply voltage (V)</td>
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<td>0.45~2</td>
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<td>Total current (nA)</td>
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<td>214 @ 0.85 V</td>
<td>214 @ 1.4 V</td>
<td>7 @ 0.45 V</td>
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<td>$V_{ref}$ (mV)</td>
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5 Conclusion

A 12.8 nA and 7.2 ppm/°C voltage reference is presented and simulated in a 0.18 µm CMOS technology. To reduce the quiescent current, all transistors are
operating in the subthreshold region and amplifier is omitted by the negative-feedback loop. Particular attention has been taken to improving the PSRR by utilizing the negative feedback technique, and an outstanding PSRR of $-79\, \text{dB}$ @100 Hz and $-56\, \text{dB}$ @1 MHz is achieved. Owning good performance, proposed voltage reference shows its superiority in applications with low-power and anti-noise constraint.

Acknowledgments

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