A closed-loop ΣΔ modulator for micromechanical capacitive sensors

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Abstract: This paper describes a CMOS fully-differential switched-capacitor (SC) single-loop Sigma-Delta (ΣΔ) modulator specialized for highly precise micromechanical capacitive sensors. This design adopts a single-loop, fourth-order, one-bit quantization architecture with feedforward paths for lower nonlinearities and power consumption. Systematic optimization is used to avoid deterioration in conversion accuracy caused by capacitor mismatch. Chopper-stabilization and double-sampling techniques are also employed to enhance performances in noise depression. Manufactured in a standard 0.35 µm CMOS process, the ASIC occupies an area of 5.32 mm\(^2\) including 25 pads. This modulator achieves a signal-to-noise ratio (SNR) of 105.2 dB and dynamic range (DR) of 113.7 dB. The whole chip consumes 12.6 mW from a 5 V supply.

Keywords: analog-to-digital conversion, Sigma-Delta modulation, chopper stabilization, micromechanical capacitive sensor

Classification: Integrated circuits

References


1 Introduction

High-accuracy analog-to-digital converters (ADCs) have been accumulating their popularity with the evolution of digital processing circuits. The main application fields range from consumer electronics to military sensors. Recently, high precision capacitive sensors have raised sustainable attention in inertial navigation and guidance, microgravity measurements in space, tilt control and platform stabilization, and GPS-aided navigators for the consumer market, all of which require high accuracy of digital output signals for weak signal detection [1]. ΣΔ modulators applied in digital MEMS capacitive sensors convert natural analog signals into digital ones for further processing [2].

In this paper, a fourth-order high-accuracy low-pass ΣΔ modulation topological structure is presented. An extra zero is designed by a novel integrator. Next, the practical circuitry design is delivered. Additionally, we give a particular analysis on the choice of the sampling capacitors as an emphasis.

2 Modulator architecture

In high-accuracy applications, non-idealities resulting from circuits leads to decrease in output precision. Therefore, single-loop topology is common in sensor fields, owning to its insensitivity to circuits’ non-idealities [3]. In this modulator, additional feed-forward paths help restrict output swing of integrators as well as reduce power consumption and harmonic distortion. As a result, a one-bit internal quantizer is enough for this design, and prevents complexity and power dissipation of a multi-bit quantizer with corresponding dynamic element matching (DEM) or any other linearization technique [4]. Besides, only quantization noise is processed in the modulation loop, which also significantly decreases the output swing of integrators and relaxes the requirements for operational amplifiers [5].

In order to gain high precision, double-sampling technique is employed. However, this causes an additional trouble of sampling capacitor mismatch, leading
to quantization noise at $f_s/2$ folding into signal bandwidth. Hence, the last integrator is designed for an extra zero at $f_s/2$, thus reducing in-band power of folded noise. The proposed modulator’s architecture is shown in Fig. 1, and gain coefficients listed in Table I.

![Fig. 1. Proposed fourth-order feed-forward low-pass modulator architecture](image1)

**Table I.** Coefficients of the fourth-order low-pass modulator

<table>
<thead>
<tr>
<th>Gain</th>
<th>$a_1$</th>
<th>$a_2$</th>
<th>$a_3$</th>
<th>$a_4$</th>
<th>$c_{11}$</th>
<th>$c_{12}$</th>
<th>$c_2$</th>
<th>$c_3$</th>
<th>$c_4$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>4</td>
<td>2</td>
<td>1</td>
<td>4</td>
<td>0.025</td>
<td>0.05</td>
<td>0.8</td>
<td>0.2</td>
<td>0.05</td>
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</tbody>
</table>

Based on the proposed architecture and coefficients, the signal transfer function (STF) and the noise transfer function (NTF) can be expressed as (1-2) below.

$$STF(z) = \frac{z^4 - 1.9z^3 - 0.06z^2 + 1.904z - 0.9352}{z^4 - 1.8z^3 - 0.12z^2 + 1.808z - 0.8704}$$  \hspace{1cm} (1)

$$NTF(z) = \frac{z^4 - 2z^3 + 2z - 1}{z^4 - 1.8z^3 - 0.12z^2 + 1.808z - 0.8704}$$  \hspace{1cm} (2)

![Fig. 2. Magnitude response of NTF](image2)

### 3 Circuit implementation

The modulator system is analyzed above and is designed to be implemented by fully differential topology, as shown in Fig. 3. Fully differential SC circuits are excellent in the fields of common-mode noise elimination, high power supply noise rejection and even order harmonic distortion exterminations. As for input signal sampling, double-sampling technique is employed to avoid high demands for operational amplifiers, due to an exorbitant sampling rate [6]. Moreover, the feedback scheme is implemented by two sampling capacitors for input signal and feedback signal, respectively. Because of less charges on the sampling capacitors,
this technique decreases harmonic distortion [3]. At the terminal of all the four integrators, we choose a passive adder composed of capacitors and switches instead of an active adder, for its high ratio of speed to power consumption [7]. Besides, chopper stabilization technique is applied to eliminate in-band low-frequency noise, especially the flicker noise in the first integrator.

In the fourth integrator, extra capacitors $C_{b1}$ and $C_{b2}$ ($C_{b1} = 3C_{14}$, $C_{b2} = C_{14}$) are used for a negative feedback. The transfer function is expressed as (3):

$$\frac{C_{S4}}{C_{14}} \cdot \frac{1}{z-1} \cdot V_{\text{in}4}(z) - \left( \frac{C_{b1}}{C_{14}} \cdot \frac{1}{z-1} + \frac{C_{b2}}{C_{14}} \cdot \frac{z}{z-1} \right) \cdot V_{\text{out}4}(z) = V_{\text{out}4}(z)$$

The output $V_{\text{out}4}(z)$ can be rewritten as (4):

$$V_{\text{out}4}(z) = \frac{C_{S4}}{2C_{14}} \cdot \frac{z^{-1}}{1 + z^{-1}}$$

According to the noise transfer function (NTF), the first integrator contributes most to the final entire noise floor, with noise of latter integrators suppressed. So the sampling capacitor of the first integrator $C_{s1}$ has to be calculated carefully. On the one hand, it is large enough to reduce the $kT/C$ noise included in the system noise level. In case of neglecting other noise except for thermal noise, the sampling capacitor $C_{s1}$ is expressed as (5):

$$C_{s1} = \frac{8DR^2kT}{V^2_{\text{ref}} OSR}$$

Since all other inevitable noises, flicker noise and quantization error, for instance, are included in practical application, $C_{s1}$ should exceed the capacitance above. However, an excessively large sampling capacitance is to increase the load of the amplifier, resulting in higher requirements for it. On the other, sampling error also comes from the on-resistance of switches in sampling loop. When the sampling period is $T_s$ and the input signal remains invariant, then the voltage in $C_{s1}$ is expressed as (6):

$$V_{\text{out}}(t) = V_{\text{in}} \left[ 1 - \exp \left( -\frac{T_s}{4R_{\text{on}}C_{s1}} \right) \right]$$

As a result, the sampling error is calculated as (7):

$$V_{\text{sa,er}} = V_{\text{in}} \cdot \exp \left( -\frac{T_s}{4R_{\text{on}}C_{s1}} \right)$$

For a modulator with an ENOB of $N$, sampling error is required to satisfy (8):

$$V_{\text{sa,er}} < 2^{-(N+1)} \cdot V_{\text{in}}$$
In consequence, $C_{s1}$ has an upper limit expressed as (9):

$$C_{s1} < \frac{T_s}{4 \ln 2 \cdot (N + 1) \cdot R_{on}}$$

(9)

As illustrated above, sampling capacitors of the first integrator are decisive to the noise floor of the whole modulator, compared to latter ones. Since there is a relatively explicit range for the sampling capacitors, we will deliver a clear contrast between performances of several modulators implemented by different choices of capacitance. There is a balance between noise level and setup-time.

Three circuits with the same modulation topology are implemented in which only the sampling capacitors ($C_1, C_2, C_3$) of the first integrators differ. The results are shown as the FFT plot in Fig. 4, where $C_3 < C_1 < C_2$. It is clear that different sampling capacitances lead to diverse distortion. Quantitatively, the three capacitors ($C_1, C_2, C_3$) lead to a SFDR of 90 dB, 81 dB, 73 dB, respectively.

4 Experimental results

The proposed fourth-order $\Sigma\Delta$ modulator was fabricated in a standard 0.35 $\mu$m CMOS technology. The chip micrograph is shown in Fig. 5. In order to obtain an obvious result of harmonic distortion, the input signal was specially designed at a low frequency of 31.25 Hz. The experimental input signal was a couple of fully differential sine waves with an amplitude of $-13.94$ dBFS. The 1048576-point FFT plot is presented in Fig. 6. Experimental results show a SNR of 105.2 dB within a 1.2 kHz signal bandwidth and an overall DR of 113.7 dB, respectively.

As a matter of conclusion, the performances are compared in Table II with some other state-of-the-art modulators in the aspect of figure of merit (FOM) which is defined as (10):

$$FOM = DR_{dB} + 10 \log \left( \frac{\text{bandwidth}}{\text{power}} \right)$$

(10)

It is crystal clear that this modulator achieves the best FOM with respect to recent $\Sigma\Delta$ designs in Table II, yet consumes more power. In the field of application areas, [8] and [11] aimed at biomedical instruments, [9] and [10] emphasized low power sensing requirements. Consequently, conversion precision is not among prior considerations in these designs. However, it does count in high-accuracy micro-mechanical capacitive sensors, especially in inertial sensors. These application requirements are also consistent with corresponding circuitry design. Concretely, a 3rd-order modulation system was employed in [10] and [11], and 1st-order, 2nd-
order in [8, 9], respectively. As a result, relatively higher noise energy caused by weaker noise shaping ability remained in signal bandwidth, leading to a $-100 \text{ dB}$, $-110 \text{ dB}$, $-90 \text{ dB}$, $-120 \text{ dB}$ noise floor in [8, 9, 10, 11], respectively. In contrast, the proposed modulator used a 4th-order modulation system to obtain an approximately $-150 \text{ dB}$ noise floor, thus conducing to a better SNR and DR. These findings further supported the idea of an extra zero reducing in-band power of folded noise. More circuit elements contributed most to higher power dissipation. Besides, outstanding performances resulting from high DC gain and slew rate in operational amplifiers were guaranteed by high current in transistors. Overall, the presented results are comparatively encouraging. Power dissipation deserves more attention in future research.

### 5 Conclusion

A 0.35 µm CMOS single-loop ΣΔ modulator for capacitive sensor interfaces has been described. Major design considerations have been discussed and employed to achieve a stable system in order to satisfy the application requirements of high precision. The entire modulator achieves 105.2 dB SNR and 113.7 dB DR.

According to the experimental results, this work satisfies all the application criteria for accelerometers and gyroscopes which are the most widely used capacitive inertial sensors.

### Table II. Performance summary and comparison

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>Bandwidth (kHz)</td>
<td>1</td>
<td>1.67</td>
<td>2</td>
<td>0.3</td>
<td>1.2</td>
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<tr>
<td>SNR (dB)</td>
<td>56</td>
<td>89.9</td>
<td>65.3</td>
<td>85</td>
<td>105.2</td>
</tr>
<tr>
<td>DR (dB)</td>
<td>-</td>
<td>96.5</td>
<td>68.2</td>
<td>88</td>
<td>113.7</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>3.3</td>
<td>1.8</td>
<td>1.6</td>
<td>1.0</td>
<td>5</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>0.0759</td>
<td>0.083</td>
<td>0.096</td>
<td>0.023</td>
<td>12.6</td>
</tr>
<tr>
<td>Process (µm)</td>
<td>0.5</td>
<td>0.18</td>
<td>0.15</td>
<td>0.18</td>
<td>0.35</td>
</tr>
<tr>
<td>FOM</td>
<td>127.2</td>
<td>169.5</td>
<td>141.4</td>
<td>159.2</td>
<td>163.4</td>
</tr>
</tbody>
</table>

Fig. 5. Chip micrograph

Fig. 6. Measured modulator output spectrum