A novel automatic attenuator with ultra-fast response time

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Abstract: This paper presents a novel automatic attenuator with ultra-fast transient response time. The proposed automatic attenuator combines control generation and a digital attenuator together. The control generation chain consists of a RF envelope detector, voltage comparators and a logic circuit. The state of the digital attenuator is determined by the output control signals of the control generation chain. The chip is fabricated using Huahong 0.18 um standard CMOS technology. Measured results are offered showing that the transient response time of the whole system is less than 10 ns in the ultra-wide operation frequency range of 1 GHz ~ 10 GHz.

Keywords: automatic attenuator, RF, ultra-wide band, integration, high speed

Classification: Integrated circuits

References

1 Introduction

Variable attenuators are widely used in many microwave systems such as phased-array radars, wireless transceivers and measure machines [1, 2, 3, 4]. Especially, digital attenuators are often applied for gain control of transceivers and temperature compensation amplifiers [5, 6]. Prior researches about digital attenuators were mainly focused on low insertion loss, large dynamic range and low insertion phase variation [7, 8, 9, 10, 11]. However, a conventional digital attenuator MMIC is usually used as an individual module of which the control voltage is provided off chip. With the tendency that integration has become more and more important due to ultra-wide frequency band of transceiver in wireless communication systems, a more integrated attenuator is demanded which can combine detection, control and attenuation together.

In this paper, an automatic attenuator is proposed. The system mainly includes an envelope detector, two comparators, a digital logic circuit and a digital attenuator. Besides, a bandgap circuit is used to provide bias currents and reference voltages on chip. The envelope detector measures the envelope of input signal. If the detection output is higher than the threshold voltage preset, the attenuator will be activated. Otherwise, the attenuator will keep at “OFF” state and input signal will pass without attenuation.

This paper is organized as follows. Section II describes the architecture of the proposed automatic attenuator. In section III, circuit design of main blocks is discussed. The measured results and conclusions are presented in section IV and V, respectively.

2 Architecture of automatic attenuator

As is shown in Fig. 1, the proposed automatic attenuator system consists of a RF envelope detector, voltage comparators, a logic circuit, a bandgap circuit and a digital attenuator. The input RF signal is divided equally into two signals by an off chip RF power splitter. Signals pass through a control chain and a digital attenuator, respectively.
The control chain generates control signals, which consists of an envelope detector, two comparators and a logic circuit. The envelope detector measures the signal’s amplitude which is then used to be compared with a reference value. The reference voltage is generated by a bandgap circuit which also provides bias for the detector and comparator circuits. Output control signals of the logic circuit are determined by the results of comparison. These control signals decide the state of the digital attenuator. In addition, two off-chip control signals, \( V_{\text{set1}} \) and \( V_{\text{set2}} \), are applied to force the digital attenuator to be the state required regardless of the RF input.

Two comparators with different reference voltages are used, as is shown in Fig. 1, in case of the ripple of the detector output, which will be discussed in detail in the following section.

3 Main circuit description

3.1 Envelope detector

The envelope detector has been well discussed in [12]. The schematic is shown in Fig. 2. The detector consists of an operational trans-conductance amplifier (OTA), a current-mirror used as a rectifying element, a buffer and an extra current source used to enhance the ability to respond to the input signal. The response time of the detector can be estimated as:

\[ t_s = \frac{5.66}{C_s C_{\text{gs}} G_0 g_m 8} \]

where \( G_0 \) is the trans-conductance of OTA, \( C_g \) the total output capacitance of the OTA and \( g_m 8 \) is the trans-conductance of M8. The transient response speed can be very fast for the proper choice of \( C_s \), \( C_g \), \( G_0 \) and \( g_m 8 \). The proposed detector can be used in an ultra-wide operation frequency range (1 GHz \( \sim \) 10 GHz) and the transient response time of the detector is less than several nanoseconds.

3.2 Comparator circuit

The comparator circuit is shown in Fig. 3. The current going through M4, M6, M8 is assumed to be \( I_a \), \( I_b \), and \( I_c \), respectively. \( V_{\text{inc}} \) is connected to the output port of the detector. In the case of \( V_{\text{inc}} > V_{\text{ref}} \), \( I_a = I_c < I_b \) because of current mirrors. The
Capacitor is charged through current $I_1$ ($I_1 = I_b - I_c$) and output voltage $V_{oc}$ increases to output a high level signal. Another situation is when $V_{inc} < V_{ref}$. $I_a = I_c > I_b$ and the capacitor is discharge through current $I_2$ ($I_2 = I_c - I_b$). $V_{oc}$ decreases consequently and outputs a low level signal. As is mentioned before, two comparators are used with different reference voltages in order to avoid the ripple of the detection output. Ripples of the detection output may cause frequent changes of the comparator output, which will eventually result in frequent flip of the control signal as shown in Fig. 4a. If there are two comparators with two different reference voltage, the output control signal can remain unchanged with proper design of logic circuit when the detection output is between two reference levels as shown in Fig. 4b.

Response time of the comparator is mainly determined by the value of load capacitor $C_L$. The next stage following comparators is a logic circuit. Therefore, the load capacitor $C_L$ of the comparator is quite small. Transient response speed can be very fast.
3.3 Logic circuit

The logic circuit generates control voltages for the digital attenuator. The schematic is shown in Fig. 5. The Karnaugh map of the logic circuit is shown in Table I. \( V_{oc1} \) is the output of the comparator with reference voltage of \( V_{ref1} \), while \( V_{oc2} \) is the output of the comparator with reference voltage of \( V_{ref2} \) (\( V_{ref1} > V_{ref2} \)) as is shown in Fig. 1. \( V1 \) and \( V2 \) are output control signals. \( V1 \) is of the opposite phase from \( V2 \). The control signal with value of 0 V is taken as “0” and the control signal with the value of 3.3 V is taken as “1”. \( V_{set1} \) and \( V_{set2} \) are external signals used to force the output control signal to be “1” or “0” regardless of the output of comparators. When \( V_{set1} \) is “0” and \( V_{set2} \) is “1”, \( V1 \) is forced to be “0” and \( V2 \) is forced to be “1” regardless of \( V_{oc1} \) and \( V_{oc2} \). In the other case, when \( V_{set1} \) is “1” and \( V_{set2} \) is “0”, \( V1 \) is forced to be “1” and \( V2 \) is forced to be “0”. If \( V_{set1} \) and \( V_{set2} \) are both “1” or “0”, output control signals (\( V1, V2 \)) depend on the output of comparators (\( V_{oc1}, V_{oc2} \)) as shown in Table I. \( Q^* \) represents that the output control signal keeps its former state.

### Table I. The Karnaugh map of the logic circuit

<table>
<thead>
<tr>
<th>( V_{set1}/V_{set2} )</th>
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<td>11</td>
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Fig. 4. Output control signal in different comparator cases

Fig. 5. Schematic of the logic circuit
3.4 Attenuator

A switched π attenuator is used in the system. The schematic is shown in Fig. 6. M1, M2 and M3 act as switches which are controlled by output control signals of the logical circuit through 5 KΩ resistors of the gate poles. High resistance can provide enough radio frequency isolation between the gate of each switched MOSFET and the control sources [9]. V1 is the control voltage for the series switch MOSFET (M1) and V2 is the control voltage for the shunt switched MOSFETs (M2, M3). The attenuator is at the “OFF” state when the control voltage V1 is 3.3 V and V2 is 0 V. In this case, the attenuator just has a small insertion loss. The attenuator is at the “ON” state when the control voltage V1 is 0 V and V2 is 3.3 V. In this case, the attenuator has the attenuation of about 25 dB. Resistance value of R1, R2, R3 can be roughly estimated according to input and output matching constraints and the attenuation value required. However, the nonlinearity of transistors and high-frequency performance of transmission lines must be taken into account. Precise value of resistors is obtained through EM simulation.

![Fig. 6. Schematic of the attenuator](image1)

4 Experiment results

The proposed automatic attenuator is implemented using HuaHong 0.18 µm standard CMOS technology. The microphotograph of the chip is shown in Fig. 7. The area including pads is 1.25 mm × 0.9 mm. The chip is wirebounded to a PCB. The test PCB board for the chip is shown in Fig. 8.

![Fig. 7. Microphotograph of the chip](image2)
An off-chip power splitter divides input RF signal into two equal signals (RFin1 and RFin2) as is shown in Fig. 1 and Fig. 8. RFin1 passes through the digital attenuator and RFin2 is the input of the detector. RFout is the output of the attenuator system. An individual test port is set to measure the output of the detector. Reference voltages (Vref1, Vref2) can be adjusted through variable resistors (RA, RB) on the PCB. Vset1 and Vset2 are external signals used to force the control signal to be “1” or “0” as is mentioned before.

Measured results of the detection output are described in detail in [12]. Fig. 9 depicts the detector’s frequency response for a constant input power equal to 1 dBm. The detection output can maintain good consistency for a constant input signal over a range of frequency from 1 GHz to 10 GHz. Fig. 10 shows the detection process. The input of the detector (RFin2) is the amplitude modulation signal with a sine-wave carrier and sinusoidal signal. The frequency of the carrier and the envelope signal is 2 GHz and 20 MHz, respectively. Results show that the detection output is successfully tracking the envelope of the input modulated signal. The delay is less than 5 ns.

Fig. 8. Test PCB board for the chip

Fig. 9. Detector frequency response
Fig. 11 shows the measured results of the control chain when the input RFin2 is a sinusoidal signal with frequency of 5 GHz. The input power of RFin2 varies from −8 dBm to 15 dBm and then changes back from 15 dBm to −8 dBm. The output control signal (V2 shown in Fig. 6) is tested through the control signal test point set in the PCB as shown in Fig. 8. The reference voltages (Vref1 and Vref2) are set to be 0.97 V and 0.87 V through variable resistors (RA, RB) on the PCB respectively. Vset1 and Vset2 are both set to be 0 V. Measured results show that input power exceeding 0 dBm will activate the attenuator and power less than −3 dBm will bring the attenuator back to be “OFF” state. The threshold power is very stable when the input frequency changes between 1 GHz and 10 GHz.

The digital attenuator is tested individually. When Vset1 is 0 V and Vset2 is 3.3 V, the attenuator is activated regardless of the RF input. The measured attenuation is
shown in Fig. 12a. The attenuator has the attenuation of 25 dB ± 2 dB. When Vset1 is 3.3 V and Vset2 is 0 V, the attenuator is at the “OFF” state and just has a small insertion loss as is shown in Fig. 12b. The attenuator has an insertion loss of 4 dB ± 1.5 dB.

An off-chip two-way broadband power divider is used to measure the transient response of the whole system. The RF input signal is divided equally into two parts (RFin1 and RFin2). RFin1 passes through the digital attenuator and RFin2 is the input of the detector. The RF input signal is an amplitude modulation signal with a sine-wave carrier and square-wave signal. The frequency of the carrier and the modulation signal is 1 GHz and 12.5 MHz, respectively. Vset1 and Vset2 are both set to be 0 V. Fig. 13 shows the measured results. The total delay of the system is less than 10 ns.

5 Conclusion

A novel automatic attenuator with very fast transient response speed is proposed in this paper. The whole system combines detection, control and attenuation together. The chip is designed using Huahong 0.18 um standard CMOS technology. Meas-
ured results show that the automatic attenuator can operate well from 1 GHz to 10 GHz and that the transient response time is less than 10 ns. In addition, the proposed architecture can be easily extended to N-bit digital attenuators. For such a performance, the automatic attenuator can be applied to many fields, such as AGC circuits or phased-array radars.