Abstract: This paper presents a design-for-test structure of charge-pump phase-locked loops for on-chip jitter measurement, in which use a voltage controlled oscillator based time-to-digital converter. The structure has four key features. 1) By employing a new PFD structure to detect the time difference, it is more suitable for detecting a wide range of timing jitter. 2) The proposed DFT circuit does not need an additional jitter-free reference signal for test using the self-refereed circuit. 3) By using a new TDC structure for on-chip jitter measurement of CP-PLL, it achieves a small test area overhead. 4) The proposed DFT structure only has a minor modification on the digital part of the CP-PLL, thus it has a little adverse influence on the circuit performance. The experiment result demonstrates its possibility of detecting a timing jitter of 0.78 ps with a measurement error of 5.78%.

Keywords: CP-PLL, design-for-test, time-to-digital converter, on chip jitter measurement

Classification: Integrated circuits

References

1 Introduction

The clock jitter of charge-pump phase-locked loops (CP-PLLs) needs to be identified to ensure correct performance of a PLL-based system. In recent years,
built-in self-test (BIST) and design-for-test (DFT) methods have been widely applied to test CP-PLLs [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22]. Among them, the most typical structure for on-chip jitter measurement is based on the time-to-digital converter (TDC). There are different kinds of TDCs often used, including those that are based on the adjustable delay line [1, 2], the tapped delay line (TDL) [3], the vernier delay line (VDL) [4, 5], the component invariant VDL [6, 18, 22], the vernier ring oscillator (VRO) [8, 9], the time-to-voltage converter (TVC) [14, 20].

The TDL TDC proposed in [3] consisted of one latch chain and one buffer chain. Input reference signal passes through a buffer and then is connected to a latch which will record the number of buffers that the signal has passed along. Thus, the circuit converts the time delay between two input signals to a certain number of steps of buffer delay. In this design, the resolution is limited by buffer delay. To increase the resolution, the VDL [4] which resolution depends on the difference between the two buffers was developed. But it is sensitive to process variations which could degrade the measurement accuracy seriously. In [6, 18, 22] the proposed component invariant VDL eliminated the effect of mismatches of various delay elements. Its resolution was limited by the frequency characteristics of D-type flip-flop. And with too much additional test circuits, it also required a large area overhead. Therefore, VRO was proposed to reduce the area [8, 9], which uses timing difference between oscillators to digitize tested signal jitter. But to eliminate process variation and reducing testing time, additional time amplifier and calibration mechanism are needed.

As shown in Fig. 1, the TVC method in [14] compared the signal under measurement with a reference signal by charging and discharging a capacitor. Firstly, the low-frequency reference signal charges the capacitor in one cycle. Then, the jitter signal discharges the same capacitor repeatedly until the voltage on the capacitor falls below a threshold. The number of times that jitter signal needs to discharge the capacitor is recorded on a binary counter. By converting the timing jitter into the voltage, it achieved high resolution. However, the additional TDC takes a large area overhead. And as the circuit detects the jitter by an XOR gate, its jitter detecting range is limited. The TVC structure used in [20] broke the limitation of XOR gate on detecting range. By using the existing voltage-controlled oscillator and the loop filter of the PLL under test as parts of the TDC, it also reduced the test area overhead. However, to measure the jitter performance of the PLL, an external jitter-free reference clock which is got difficultly was needed.
Thus, a self-refereed DFT structure of CP-PLL for on-chip jitter measurement which use a TDC based on TVC with auto-calibration technique is proposed in the paper. In the design, several factors like the testing time, the resolution, the test area overhead, the measurement accuracy and its effects on the performance of circuit under test will also be carefully considered. Results indicate that the proposed structure achieves a high resolution with small area overhead. The measurement accuracy, the test time and its effects on the performance are also acceptable.

2 Circuit design

2.1 The proposed self-refereed DFT structure

Fig. 2 shows the basic architecture of CP-PLL. It contains five units: phase/frequency detector (PFD), charge-pump (CP), loop filter (LF), voltage controlled oscillator (VCO), divide-by-N (DBN). The PFD detects the phase and the frequency difference between the feedback signal clk.out and reference signal clk.ref, and converts it into two digital signals, i.e., Up and Down. Then the CP combined with LF transform these two signals into an analog voltage $\Delta V$ for the VCO. Finally, the VCO delivers output signal, whose frequency is changed with the analog voltage $\Delta V$ inputed to it and is then shifted to the input dynamic range by DBN. The frequency variation yields the phase difference, thus we can record the frequency variation to get time difference between the feedback signal and reference signal.

![Fig. 2. The basic architecture of CP-PLL.](image)

Fig. 3 shows the proposed DFT structure. It uses the existing CP-PLL combined with a counter as TDC, in which the CP-PLL converts time difference $\Delta T$ into a frequency variation $\Delta f$. Then by counter, the frequency variation $\Delta f$ will be transformed into count difference $\Delta N$. Thus, the time difference $\Delta T$ can be obtained from the count difference $\Delta N$, as shown in Eq. (1), where $I$ is the current of charge pump (CP) and $C$ is the capacitance of loop filter (LF), $K$ is the gain of VCO, $N$ is the dividing coefficient at the access location of the counter, $T$ is the test time and the parameter $k$ represents the jitter measurement resolution.

$$\Delta f = K \times \frac{I}{C} \times \Delta T, \quad \Delta N = \frac{\Delta f}{K} \times T \Rightarrow \Delta T = k \times \Delta N, \quad k = \frac{C \times N}{K \times I \times T}. \quad (1)$$

A self-refereed (S-R) circuit is added in the CP-PLL design stage to calibrate the jitter measurement resolution of the proposed TDC and control the working state of CP-PLL. To avoid the limitation of XOR gate on detecting range existing in the conventional TDC approach shown in Fig. 1, there is also a minor modification of the PFD in the CP-PLL. Because the modification is mainly at the PFD part of the CP-PLL, its influence compared to a traditional PFD will be evaluated. Time
delay caused by the new PFD structure and the S-R unit compared to the traditional
PFD structure is about 100 ps level and all these minor modifications on the digital
part of the CP-PLL will be added in the design stage. Thus the additional delay
created by it can be incorporated in the original loop characteristics. The access
location of the counter can be selected according to the requirements. In the paper,
the counter is connected to the second stage of DBN to shorten the test time and
avoid the influence on the performance of CP-PLL.

This DFT structure employs the whole CP-PLL as one part of TDC. The CP-
PLL converts the phase difference into a frequency variation. Then by the addi-
tional counter, the proposed structure can change the phase difference into count
difference. Using only one path to measure timing jitter instead of matching the two
delay chains, this method is less sensitive to the process variation effects. To avoid
the loading effect at analog node, the additional test circuits is all digital and only
access the digital node of CP-PLL, thus it has a little influence on the circuit
performance.

As shown in Table I, the proposed DFT structure has three working modes. In
normal mode, the signal rst is set to be logic high. It works as a CP-PLL with the
counter being disabled. In jitter measurement mode, the signal rst is set to be logic
low and the signal cal is set to be logic high. It keeps working on the first state until
the CP-PLL is locked in. And then it will be used to detect the timing jitter between
the reference signal and feedback signal of the CP-PLL. In calibration mode, the
signal rst is set to be logic low and the signal cal is set to be logic low. In order to
make sure the accuracy of the approach, it still firstly works as a CP-PLL to get
locked in. That is to make the initial state of the circuit is at the same state as in the
jitter mode as possible. Then it will be used to detect a known time difference to get
the jitter measurement resolution.

<table>
<thead>
<tr>
<th>Table I. The working modes of proposed DFT structure</th>
</tr>
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<tbody>
<tr>
<td>rst</td>
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<tr>
<td>-----</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>0</td>
</tr>
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</table>
2.2 The S-R unit

The jitter measurement resolution of the proposed TDC should be calibrated. As shown in Eq. (1), the resolution $k$ depends on all the key parameters associated with CP-PLL and the test time $T$. Due to the leakage current, the supply immunity decoupling and the self generated noise, the resolution $k$ is not a fixed value even all the parameters have been decided. The calibration of $k$ includes two steps, deciding the range of the test time $T$ and using an accurate time difference to calibrate the TDC.

1) Deciding the test time $T$.

Supposed the required measurement resolution is $k_0$, then the range of $T$ can be decided by Eq. (2).

$$k = \frac{C \times N}{K \times I \times T} \leq k_0 \Rightarrow T \geq \frac{C \times N}{K \times I \times k_0}.$$  \hspace{1cm} (2)

2) Getting an accurate time difference to calibrate the TDC.

Fig. 4 shows the schematic of the proposed S-R unit, in which two DFFs are used to get a signal delayed by one clock period $\Delta T_0$ of the reference signal.

In the calibration mode, firstly the reference signal and the feedback signal will be input to the CP-PLL. The durations of this time should be longer than lock-in time of the CP-PLL and the settling time of the LF, so that the CP-PLL can track the phase of the reference clock and finally keep lock-in state. Then the reference signal and its delayed signal will be input to the CP-PLL and the counter will be enabled. Supposed the count of the counter in test time $T$ is $N_{\Delta T_0}$, the relationship between $\Delta T_0$ and $N_{\Delta T_0}$ can be obtained as

$$\Delta T_0 = k \times \left( N_{\Delta T_0} - \frac{T}{\Delta T_0} \times N \right).$$  \hspace{1cm} (3)

Where $N$ is the dividing coefficient at the access location of the counter, $\Delta T_0$ represents one clock period of the reference signal. Here we do not consider the delay of logic gates used in the S-R unit, which is at $10 \times 10^{-12}$ s level and much less than the value of $\Delta T_0$. Because the S-R circuit get the accurate time difference in an external environment affected by noise, temperature and process, to reduce the measurement error, the calibration process will be repeated $n$ times. At each time, the count of the counter will be recorded as $N_{\Delta T_{01}}, N_{\Delta T_{02}}, \ldots, N_{\Delta T_{0n}}$. Then the resolution can be obtained using the Eq. (4). Thus, the proposed DFT circuit does not need an additional jitter-free reference signal for test using the S-R circuit.

![Fig. 4. The structure of the S-R unit.](image-url)


\[ k = \frac{\Delta T_0}{\left( \frac{N_{\Delta T_0} + N_{\Delta T_{in}} + \cdots + N_{\Delta T_{in}}}{n} - \frac{T}{\Delta T_0} \times N \right)} \]

2.3 The proposed PFD

As shown in Fig. 5, a new PFD structure consisting of two cascaded DFFs is used. Before the CP-PLL being locked in, both of two cascaded DFFs are used to allow the CP-PLL to track the phase of the reference signal. Then when the CP-PLL is in locked-in state, there will be a time difference \( \Delta T \) between the reference signal and the feedback signal. A reset signal Rst is added to the first two DFFs to disable it, which will transform the two repeated input signals into two single pulse signals, so that the time difference \( \Delta T \) will be locked-in. Then the second two DFFs continue working to detect the time difference for the jitter measurement. Because the dead zone of the PFD is zero, this structure is especially suitable for detecting the timing jitter which is too little or too large.

To clarify the working process of the jitter measurement, Fig. 6 shows the timing behavior of the PFD. When in calibration mode, the calibration signal cal is set to logic low, the PFD is firstly used to detect the phase difference between the reference signal clk_ref and the feedback signal clk_test and then to detect the timing jitter between the reference signal clk_ref and the signal delayed by one clock period of it after the CP-PLL being locked in. When in jitter measurement mode, the calibration signal cal is set to logic high, the PFD is also firstly used to detect the phase difference between the reference signal clk_ref and the feedback signal clk_test and then to detect the timing jitter between them after the CP-PLL being locked in.

The proposed DFT structure can detect a wide range of timing jitter between the two clocks by using this PFD, which is implemented using two edge triggered resettable D flip-flops. As shown in Fig. 6. Even if the phase difference of the two inputs is nearly zero, the up and dn signals still have short pulses to turn on the transistors of CP. The difference between their pulse widths represents the phase difference. Thus, a zero dead zone is achieved. However, if there is a constant phase offset between clk_ref and clk_test, the phase offset can also be measured and separated from the jitter by observing the histogram of the time differences. The mean in the histogram represents the phase-offset error, but the jitter is measured by the variance.
3 Experimental results

Fig. 7 shows the chip micrograph of the proposed structure. The chip is implemented using TSMC 0.13-µm CMOS technology. The chip occupies a die size of approximately $540 \times 580 \mu m^2$. Comparing the area with and without the DFT circuits reveals that the area overhead is about 17.2%.

(a) When signal cal=0.

(b) When signal cal=1.

Fig. 6. Timing behavior of the proposed PFD.

Fig. 7. The chip micrograph of the proposed structure.
Table II. Test chip characteristic summary

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Value</th>
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<tbody>
<tr>
<td>Reference clock</td>
<td>25 MHz</td>
</tr>
<tr>
<td>VCO frequency</td>
<td>1.6 GHz</td>
</tr>
<tr>
<td>Current of CP</td>
<td>120 μA</td>
</tr>
<tr>
<td>Gain of VCO</td>
<td>41.8 MHz/V</td>
</tr>
<tr>
<td>Capacitance of LF</td>
<td>85 pF</td>
</tr>
<tr>
<td>Coefficient of DBN</td>
<td>64</td>
</tr>
<tr>
<td>VCO CMOS technology</td>
<td>0.13-µm</td>
</tr>
<tr>
<td>VDD</td>
<td>1.8 V</td>
</tr>
<tr>
<td>Power consumption</td>
<td>14.7 mW</td>
</tr>
<tr>
<td>Area</td>
<td>0.32 mm²</td>
</tr>
<tr>
<td>RMS jitter</td>
<td>4.679 ps</td>
</tr>
<tr>
<td>Peak to peak jitter</td>
<td>28.75 ps</td>
</tr>
</tbody>
</table>

The characteristic summary of CP-PLL is shown in Table II. In the paper, supposed \( k < 1 \) ps, then according to the Eq. (5).

\[
k = \frac{85 \times 4}{41.8 \times 120 \times T} < 1 \Rightarrow T > 0.0678 \text{ s}.
\]  

(5)

Here the test time \( T \) is designed to 50 ms.

Fig. 8. Histogram of the DFT output in calibration mode.

Fig. 9. Histogram of the DFT output in jitter measurement mode.

A 40 mV 50 MHz sinusoidal noise is injected into the input power supply of the circuit to verify the effectiveness of the DFT circuits in harsh environments. It can be replaced by other noises or removed. The results will not be affected. Fig. 8 shows the DFT output in calibration mode. The histogram is made up of 12000 hits. The average value of the output results is calculated at 51000. The value of \( \Delta T \) is \( 4 \times 10^{-8} \) s, which is one clock period of the reference signal. Thus the resolution \( k \) is obtained from the Eq. (6).
The delay of logic gates used in the S-R unit is not considered here, which is at 10 ps level. As $10 \times 10^{-12}/51000 \approx 2 \times 10^{-4}$ ps $\ll 0.784$ ps, its influence is negligible.

Each output value of the DFT structure represents a time difference equivalent to the resolution $k$ between the reference clock and the feedback clock. Thus the jitter value can be got by simply multiplying the output results of the DFT in the jitter measurement mode by 0.784 ps. Fig. 9 shows the PDF histogram of the DFT output in the jitter measurement mode. Thus the RMS jitter of the CP-PLL measured by the DFT circuit in this case is $6.3004 \times 0.784 = 4.9395$ ps. Fig. 10 shows the timing jitter measured using a Tektronix MSO71254C mixed-signal oscilloscope. The RMS jitter is 4.679 ps. The measurement error is about 5.78%.

The performance comparison between two CP-PLLs with and without the added DFT circuits is shown in Fig. 11. It indicates that the locking time for the CP-PLL with and without the added BIST circuits are 5.15 us and 4.77 us respectively. Thus the additional DFT circuits have a little influence on the circuit performance.

The results comparison is presented in Table III. Compared with others, the proposed DFT structure gets a relatively high resolution of 0.78 ps with a measurement error of 5.78% which is acceptable for the test application. What's more, the proposed structure does not need the external jitter free clock signal for jitter measurement.
4 Conclusion

This paper presents a self-refereed DFT structure of CP-PLL for on-chip jitter measurement. By using the S-R circuit, the proposed DFT circuit does not need an additional jitter-free reference signal for test. By employing the existing circuits of CP-PLL as one part of the proposed TDC, it has a small test area overhead. In the design, the additional test circuits is all digital and only access the digital node of CP-PLL, thus the proposed structure has a little influence on the circuit performance. A new PFD structure consisting of two cascaded DFFs circuits is also used to break the limitation of XOR gate on detecting range. Thus the proposed structure can detect the timing jitter which is too little or too large. The experiment results show a relatively high resolution of 0.78 ps with an acceptable measurement error of 5.78% for the test application.

![Fig. 11. The control voltage of VCO.](image)

<table>
<thead>
<tr>
<th>Reference</th>
<th>[8]</th>
<th>[9]</th>
<th>[20]</th>
<th>[22]</th>
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<td>65</td>
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<td>180</td>
<td>130</td>
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<td>-VRO</td>
<td>-TVC</td>
<td>-VDL</td>
<td>-TVC</td>
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<tr>
<td>Frequency (GHz)</td>
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<td>0.5</td>
<td>1.6</td>
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<tr>
<td>Test time</td>
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<td>long</td>
<td>3.44 s</td>
<td>&gt;67 ns</td>
<td>50 ms</td>
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<td>27%</td>
<td>36.7%</td>
<td>59%</td>
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<tr>
<td>Self-refereed</td>
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<td>Y</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Resolution (ps)</td>
<td>1.8</td>
<td>152.9</td>
<td>1.17</td>
<td>6</td>
<td>0.78</td>
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<tr>
<td>Oscilloscope (RMS)</td>
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<td>1903 ps</td>
<td>5.45 ps</td>
<td>10.36 ps</td>
<td>4.67 ps</td>
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<tr>
<td>DFT (RMS)</td>
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<td>1987 ps</td>
<td>6.25 ps</td>
<td>9.09 ps</td>
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<tr>
<td>Error (%)</td>
<td>8.9</td>
<td>4.4</td>
<td>14.6</td>
<td>12.3</td>
<td>5.78</td>
</tr>
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</table>

*represents simulation results. **with a pulse amplifier.
Acknowledgements

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