An ultra-low-power 2.4 GHz RF receiver in CMOS 55 nm process

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Abstract: This paper presents a 2.4 GHz ISM-band wireless receiver suitable for ultra-low-power (ULP) operation. In this design, a sliding-IF receiver architecture is adopted for achieving desired noise performance with low power consumption. Moreover, a new circuit design method is proposed for achieving ULP design. Some low power circuit techniques such as inverter based amplifier, current reuse and sub-threshold biasing techniques are presented in the design. The proposed receiver is designed and fabricated in a standard 55 nm CMOS process. The measurement results show a voltage gain of 29.2 dB, a noise figure (NF) of 6 dB and third-order intercept point (IIP3) better than -20 dBm. The receiver consumes 2.4 mW from a 1.2-V supply. The core area of the receiver is 0.5 mm^2 .

Keywords: CMOS, ultra-low-power, receiver, ISM-band

Classification: Integrated circuits

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1 Introduction

With the gradual maturation of wireless sensor networks and Internet-of-Things (IoT), short-range ultra-low-power (ULP) wireless connectivity has been widely researched [1, 2]. 2.4 GHz ULP wireless products compliant with the existing wireless standard such as the IEEE 802.11, Bluetooth and covering the global ISM band, will be of great demand. As one of the key subsystem for wireless sensor networks and IoT, ULP receivers impose stringent requirements on cost, power consumption and performance.

To date, numerous works have been done to attain low power consumption [3, 4, 5, 6], and there are lots of methods to achieve low power, such as sub-threshold region biasing, current reuse, and g_m -boosting techniques. By applying this methods, current and noise figure (NF) of the receiver can be reduced. But only one technique in circuit level is not good enough to achieve ultra-low power consumption. Therefore, some novel methods in architecture have been proven meaningful. Most conventional low power receivers have used simple architectures such as super-regenerative and sub-sampling receiver. Although a sub-sampling receiver using passive high-Q resonators consumes very low power, they require rather expensive passive components, such as FBARs and RF-MEMS and area cost is huge. As for high data-rate and low cost application, low power application, standard CMOS homodyne or super-heterodyne RF receivers are preferred. In

recent years, Sliding-IF architecture, as an effective method to save whole receiver power consumption because it does not require a power-hungry LO generation, is widely applied in ULP receiver design [7, 8].

In this paper, we present an ULP CMOS 2.4 GHz receiver combining low power circuit techniques and a sliding-IF architecture, with the objective of minimizing power consumption while achieving the required performance. Section 2 briefly addresses the receiver architecture. Section 3 proposes a new circuit design method for ULP. Section 4 describes the circuit in detail. Section 5 presents the measurement results followed by the conclusions in Section 6.

2 The ULP receiver architecture

The sliding-IF architecture is commonly deployed for ULP receiver with advantages such as low LO conversion frequency, high image rejection, and low implementation cost [9]. The proposed receiver is designed for use in a sliding-IF architecture, as shown in Fig. 1. The RF signal is down-converted to baseband through two-step mixing. The PLL is locked at $4/5$ of the input center frequency (e.g., $f_C = 2.5$ GHz) as the LO of the RF mixer (e.g., $f_{LO1} = 2$ GHz). Then it is further divided by 4 (e.g., $f_{LO2} = 500$ MHz) to provide a 4-phase LO for the IF mixer with a 25% duty-cycle LO generator. With this frequency plan, the image frequency is located at $1/5$ of the RF frequency far away from the RF frequency, and the image signal can be easily rejected by the external antenna and input matching network. The quadrature passive IF mixer combine with transimpedance amplifier (TIA) is applied for further compressing image signal and achieving good linearity performance. Otherwise, in the receiver architecture, an intermediate g_m -stage between the RF mixer and IF mixer is eliminated, which boost the input third-order intercept point (IIP3) of the whole receiver in an effective way.

Fig. 1. Block diagram of proposed receiver.

The data rate is critical to the efficiency of the design. With a very high data rate the receiver consumes a large amount of power and bandwidth, whereas a low data rate requires the transceiver to stay on for longer duration transmitting the same amount of data. Specifications will vary with the specific applications, and the Bluetooth standard provides an example of typical requirement for a low-power

radio. A data rate of 1 Mbps, according to 2.4 GHz ISM-band Zigbee standard, is assumed to be sufficient for most application involving wireless data transfer. Based on a bit error rate (BER) of 0.1% and minimum sensitivity requirement (-94 dBm), the required specifications of the RF receivers can be derived with GFSK modulation scheme, as shown in Table I.

Table I. Specification of the RF receiver

Specification	Target
Voltage gain (dB)	30
LO amplitude (mV _{p-diff})	200
IF amplitude (mV)	0.3~10
Noise figure (DSB) (dB)	6
IIP3 (dBm)	-22
DC Current (mA)	2

3 A new circuit design method for ULP

3.1 Inverter based LNA

To achieve ultra-low-power performance, the inverter-based amplifier architecture with sub-threshold biasing technique is used in the low noise amplifier (LNA). The proposed LNA is shown in Fig. 2(b). Compared to conventional LNA architecture shown in Fig. 2(a), this architecture contains current reuse and its effective transconductance g_m is equal to the sum of the transconductance of M_1 and M_2 , that means less DC current is needed for achieving a target gain.

Fig. 2. (a) Conventional LNA architecture, (b) Inverter based LNA architecture.

The simulation results of the conventional and the inverter based LNA are shown in Table II. The operational frequency is set to 2.4 GHz, and all of the used components including transistor, inductor and capacitor are chosen from a standard 55 nm CMOS process and the parasitic effect of package are taken into consideration. As we can see, the inverter based LNA consumes less current for achieving a target noise figure. Moreover, an on-chip RF choke inductor is not needed in the inverter based LNA.

Table II. Comparison of the conventional and inverter based LNA

	Conventional LNA	Inverter based LNA
DC current (uA)	680	520
Voltage gain (dB)	17.6	18
DSB NF (dB)	3.2	3.2

3.2 A new subthreshold design method

As usual, when V_{GS} is smaller than or near to V_{TH} , the NMOS transistors are considered to be cut off. In fact, when $V_{GS} < V_{TH}$, drain current I_D is finite, but it exhibits an exponential dependence on V_{GS} , which is different from the square law. So compared with saturation region, the transconductance g_m will be boosted under the same current bias. Aiming at sub-threshold biasing technique, a new ULP design method to find the sweet biasing point of the MOSFETs is proposed in this paper. Taking the technology cutoff frequency f_T and the tradeoff between circuit performance and current consumption into consideration, a new figure of merit (FOM) about the g_m , f_T and I_D of the transistor is specified as equation (1), which is different from the conventional FOM definition (e.g., $FOM_1 = g_m \cdot f_T / I_D$).

$$FOM_2 = \frac{g_m \cdot \sqrt{f_T}}{I_D} \quad (1)$$

To emphasize the advantages of the new FOM, Fig. 3(a) depicts the simulated FOM_1 and FOM_2 of a single NMOS transistor in a 55 nm CMOS technology of Fujitsu. In addition, the drain current per unit gate and f_T are also plotted in the figure. The device features a 16 $\mu\text{m}/60\text{ nm}$ with 4 fingers. This curves figure out that FOM_2 is maximized at $V_{GS} = 500\text{ mV}$ while FOM_1 is maximized at $V_{GS} = 600\text{ mV}$ (with $V_{TH} \approx 600\text{ mV}$). The drain current per unit gate width at the maximum points of FOM_1 and FOM_2 are 92 $\mu\text{A}/\mu\text{m}$ and 36 $\mu\text{A}/\mu\text{m}$ respectively.

Fig. 3. (a) FOM_1 and FOM_2 versus V_{GS} , (b) NF_{min} and G_{msg} versus V_{GS} .

Let's analyze the key circuit performance, the minimum noise figure NF_{min} and maximum stable power gain G_{msg} . By sweeping the allowable unit width sizes ($w = 4\text{ }\mu\text{m}, 3\text{ }\mu\text{m}, 2\text{ }\mu\text{m}, 1\text{ }\mu\text{m}$), with fixed total width of 24 μm , fixed gate length of 60 nm, variable number of fingers ($f = 6, 8, 12, 24$), the simulated NF_{min} and G_{msg} versus V_{GS} are presented in Fig. 3(b). From the simulation results, on one hand,

NF_{min} is considerably low of less than 0.3 dB for $V_{GS} > 0.4$ V and varies 0.07 dB with different fingers, that means moderate noise figure target is achievable under sub-threshold region. On the other hand, G_{msg} is dependent on V_{GS} under sub-threshold biasing in general, but is larger than 17 dB at $V_{GS} = 0.5$ V and can be boosted further with applying inverter-based topology. Furthermore, G_{msg} is sensitivity to transistor's unit width and the number of fingers. At $V_{GS} \geq 0.5$ V, including sub-threshold region and saturation region, the variation of G_{msg} is up to 3 dB under the same total width, different fingers and unit width. Therefore, by biasing the transistors at the sweet point of FOM_2 and carefully choosing the fingers and unit width of transistors, the MOSFET can perform a LNA characteristic. In addition, a comparison of the simulation results of the FOM_1 and FOM_2 is shown in Table III.

Table III. Comparison of the FOM_1 and FOM_2 design methods

	Conventional FOM_1	Proposed FOM_2
I_{DD} (uA)	1472	576
G_{msg} (dB)	21.7	19.4
NF_{min} (dB)	0.16	0.19
FOM	434.8	719.9

In LNA design, the three most important characteristics are voltage gain (A_v), noise figure (F) and power consumption and combined in equation (2) [10]. This FOM is applied to evaluate the proposed design method.

$$FOM = \frac{Av_{abs} \cdot freq_{GHz}}{(F_{min} - 1)_{abs} \cdot (I_D \cdot Vdd)_{mW}} \quad (2)$$

From the Table III, with the proposed FOM_2 design guidance, the DC current consumption is only 39% of the DC current that followed the conventional FOM_1 , and the voltage gain and minimum noise figure performance is a little bit worse than that followed FOM_1 . On the FOM evaluation, the proposed FOM_2 is much higher than the conventional FOM_1 , which reveals a considerably large current saving is achieved in the proposed design method. Analyzed from physical characteristic, as the semiconductor manufacturing process technology advances, the intrinsic cutoff frequency f_T of MOSFET is improved. For 55 nm CMOS process, the f_T is larger than 100 GHz at $V_{GS} = 0.5$ V (sub-threshold region) and increased rapidly with V_{GS} . Thus, for sub 5 GHz RF circuit design, the restriction of f_T is puny in reality, and sub-threshold biasing is workable in ULP design. In comparison to conventional FOM_1 , the proposed FOM_2 weakens f_T , and provides an effective guidance for ULP design in the advanced CMOS process.

4 The proposed circuit implementation

4.1 The proposed LNA and RF mixer

A single-ended LNA is applied for its low power consumption and to avoid an on-chip balun. In order to decrease crosstalk and instability, deep N-well NMOS transistor is used in LNA. Otherwise, P type and N type guard ring are both added in the layout to prevent latchup. As for RF mixer, traditional single-balanced mixers

are not favored due to the large LO feedthrough, but using a pseudo differential double balanced mixer with one of the inputs being AC-grounded suffers from the 50% waste of power and transconductance, thus, resulting in a serious degradation of the noise performance and efficiency. Aiming at this issues, a push-pull mixer is proposed to improve both noise performance and current efficiency. Thus, a combination of the inverter based LNA and push-pull RF mixer are proposed as shown in Fig. 4, and the specifications are classified in Table IV.

Table IV. The specification of the LNA and RF mixer

	LNA	Mixer
I_{DD} (uA)	520 uA	660 uA
Voltage gain (dB)	18	4
NF_{min} (dB)	3.2	8
IIP3 (dBm)	-12	3

Fig. 4. The schematic of the proposed LNA and RF mixer.

In the schematic, an off-chip inductor L_G is used for the input resistance matching, and the input impedance of the LNA can be expressed as equation (3).

$$Z_{in} = \frac{1}{j\omega(C_P + C_{GS_{eq}}) + \frac{1 + g_{m_{eq}} \cdot Z_{out}}{Z_{eq_{fb}} + Z_{out}}} + j\omega L_G \quad (3)$$

Where $C_{GS_{eq}}$ is the equivalent gate-source capacitance of the transistors M_1 and M_2 , $g_{m_{eq}}$ is the equivalent transconductance of M_1 and M_2 , $Z_{eq_{fb}}$ represents the equivalent feedback impedance between the point A and B and $Z_{eq_{fb}} = 1/Y_{eq_{fb}}$, Z_{out} is the load resistance of the LNA. The parallel capacitor C_P is added for tuning the real part, and the imaginary part of the input impedance is neutralized by tuning the series inductor L_G . At input impedance matching, the equivalent voltage gain of the LNA can be expressed as

$$|A_V| \cong \left| \frac{(Y_{eq_fb} - g_{m_eq}) \cdot Z_{out}}{1 + Z_{out} \cdot Y_{eq_fb}} \right| \quad (4)$$

The minimum noise factor (F_{min}) of the LNA is derived at (5), where g_{ds_eq} represents the drain-source impedance of M_1 and M_2 , R_{G_eq} is the total gate series resistance. The equation assumes the biasing resistance can be negligible in noise calculations for its high value. The boosted transconductance ($g_m = g_{mp} + g_{mn}$) results to a lower noise figure and low power consumption.

$$F_{min} = 1 + \frac{g_{ds_eq} \cdot Z_{out} + R_{G_eq} \cdot Av^2}{Av^2 R_S} \quad (5)$$

As for the push-pull mixer, on one hand, a lossless single-to-differential conversion is provided inherently, on the other hand, the current reuse is contained in the structure. The linearity performance (e.g., IIP3) of the mixer is improved by the complementary input stage [11]. The LO signal's amplitude of larger than 200 mV with differential inputs is needed and provided by an on-chip phase lock loop (PLL). Through the switch stage consisting of the complementary NMOS and PMOS transistors (M_5 , M_6 , M_7 and M_8), the LO feedthrough can be canceled. Moreover, for keeping the IF dc voltage of 600 mV, a common-mode feedback (CMFB) path is applied between the output and the bias terminal of PMOS (M_4) as shown in Fig. 4.

Fig. 5 shows the simulated input and output signal spectrum of the proposed RF mixer. The input LO and RF frequency are located at 2 GHz and 2.5 GHz respectively. After downconversion, the output IF signal frequency is at 0.5 GHz. Simulation shows that 2 GHz LO feedthrough can be suppressed by 35 dBc and of lower than 5 mV, which is easy to be filtered out by the following stage. The RF mixer only consumes 660 μ A DC current from a 1.2 V supply voltage.

Fig. 5. (a) The Input spectrum, (b) Output spectrum of the RF mixer.

4.2 Passive IF mixer

The output signal of the RF mixer is further down-converted with a traditional passive quadrature IF mixer which is adopted for its low flicker noise and better linearity performance [12]. The IF mixer is implemented with a 25% duty-cycled LO generator to avoid the noise leakage from the other channel. Two transimpedance amplifiers are integrated to convert the output current signal to voltage

signal, which is based on operational transconductance amplifier (OTA). For low power consideration, sub-threshold biasing technique is also applied in the OTAs. The IF mixer consumes 680 μ A current from a 1.2 V supply voltage.

5 Measurement results

The proposed ultra-low-power receiver has been fabricated with 55 nm CMOS technology and consumes only 2 mA from 1.2 V supply. The chip micrograph is shown in Fig. 6(a), which occupies 0.5 mm^2 , excluding the pads. The PCB test board is shown in Fig. 6(b). During the design process, off-chip components, package model, bond wire model and PCB trace model are included in the simulation. With careful and accurate post-layout simulation, the measurement of the receiver achieves a uniform result as the simulation.

Fig. 6. (a) The chip micrograph. (b) The test board of the proposed receiver.

Fig. 7(a) shows the measured return loss of the receiver that the S11 of less than -10 dB is achieved over $2.37\text{--}2.45 \text{ GHz}$. With fine tuning the off-chip inductor L_G , the return loss can be adjusted. In Fig. 7(b), the measured IM3 characteristics are plotted. In the IIP3 measurement, the two-tone RF input signals are set to 2.401 GHz and 2.4012 GHz respectively, and the LO is set to 1.92 GHz . After down-conversion, the first-order signals are at 1 MHz and 1.2 MHz , and the third-order intermodulation signals are at 0.8 MHz and 1.4 MHz . From the figure, the IM3 rejection of larger than -50 dBc , and the IIP3 of -20 dBm are achieved at

Fig. 7. (a) S11 of the receiver. (b) IM3 characteristic of the receiver.

the maximum gain operation. The very low current degrades the linearity of the receiver that is not compensated by the extra circuits and gain lessening. However, during the design, an intermediate g_m -stage between the RF mixer and IF mixer is eliminated, which boosts the IIP3 to a certain extent.

As shown in Fig 8(a), NF of less than 6.5 dB is measured in the concerned IF frequency range from 10 kHz to 1 MHz at maximum gain operation. For a given quality factor of input matching network, minimum NF of LNA can be achieved by optimizing the width of transistors M_1 and M_2 . With appropriately gain planning and delicate design in architecture, the NF of the receiver is optimized to an outstanding level. In Fig. 8(b), a 29.2 dB maximum voltage conversion gain is achieved. In the gain measurement, the input power of the LO and RF signals are set to -10 dBm and -70 dBm respectively. For measuring the RF bandwidth characteristic, the RF frequency is tuned from 2.401 to 2.501 GHz with the LO frequency tuned from 1.92 to 2 GHz ($4/5$ of the RF frequency) synchronously, and IF frequency is fixed at 1 MHz. With fine tuning the input matching, a 0.6 dB gain error is measured at the whole band.

Fig. 8. (a) NF of the receiver. (b) Conversion gain of the receiver.

The receiver performances are summarized in Table V together with other state-of-art receivers. It can be seen that compared with other ULP 2.4 GHz receivers, this work achieves low NF and moderate linearity performances while consuming low power and small area cost.

Table V. Performance summary and comparison

	Ref. [13]	Ref. [3]	Ref. [14]	Ref. [15]	This work
CMOS Technology	65 nm	180 nm	65 nm	28 nm	55 nm
Supply (V)	0.3	1	1.2	1	1.2
Frequency (MHz)	2400	2400	2400	2400	2400
Gain (dB)	83	17.5	57	NA	29.2
DSB NF (dB)	6.1	10.2	8.5	6.5	6
IIP3 (dBm)	-21.5	-13	-6*	-19	-20
Core area (mm ²)	2.5	0.052	0.24	1.9	0.5
Power (mW)	1.6	0.83	1.7	2.75	2.4

*Out-band measured result

6 Conclusion

In this paper, an ultra-low-power 2.4 GHz ISM-band wireless receiver fabricated in a standard 55 nm CMOS process is proposed. A new design method for ULP circuit design is proposed and the analysis of system and circuit level design are both presented. The measurement results show that 6 dB NF, –20 dBm IIP3 and 29.2 dB voltage gain are achieved with power consumption only 2.4 mW from 1.2 V supply. The core area of the receiver is only 0.5 mm².

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