Design of low-loss 60 GHz integrated antenna switch in 65 nm CMOS

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Abstract: A 60 GHz antenna switching architecture is presented for millimeter-wave transceivers. This circuit topology re-uses the last stage’s transistor of power amplifier (PA) and the first stage’s transistor of low-noise amplifier (LNA) as switches, and the matching blocks. A two-stage LNA and a two-stage PA are designed considering antenna switching operation in 65 nm CMOS. The method has lower loss than conventional switches in receiver mode. The most important advantage is no additional area penalty compared to conventional methods. 2.9 dB minimum noise figure (NF) in the receiver mode is measured, and 2 dBm of OP_{1dB} is measured in the transmitter mode.

Keywords: CMOS, mm-wave, MIMO, TX/RX switch, phased arrays

Classification: Microwave and millimeter-wave devices, circuits, and modules

References

1 Introduction

60 GHz millimeter-wave (mm-wave) region gets more attention due to larger available bandwidths [1, 2, 3]. Transmit/receive switch for a mm-wave multi-Gb/s system is an advantageous block when considering phased array and multi-input multi-output (MIMO) communication for sharing antennas [3, 4, 5, 6, 7, 8, 9, 10, 11]. It is crucial to decrease the silicon area consumption of switch, while, also, care should be taken for noise figure (NF) of receiver (RX), and linearity of transmitter (TX). Although there are other topologies for switch architecture [3, 10, 11], the common topology for antenna switch is based on quarter-wavelength ($\lambda/4$) [4, 5, 6, 7, 8]. The conventional switches have long $\lambda/4$ length (typically 600 to 700 µm in standard CMOS) transmission lines (TLs) which consumes relatively large area on-chip and introduce loss especially in mm-wave frequency region. For instance, the switch in [5] has one of the best performance in terms of loss in the literature. However, the area of the switch is 0.275 mm² and for an 8 × 8 MIMO system, 8 of this switch would consume a total area of 2.2 mm². Considering advanced manufacturing nodes, this would result in increased cost for silicon. A small area switch is presented in [3] based on balun architecture consuming a total area of 0.024 mm². Nevertheless, this topology has higher loss which affects the overall TX-to-RX communication performance. In here, an integrated antenna switch with PA and LNA is proposed and the concept is illustrated in Fig. 1(a). Here, a 60 GHz antenna switch is presented with no additional area consumption and low-loss, by re-using the last stage’s transistor of PA and first stage’s transistor of LNA and the matching blocks.

Next section presents the design and analysis of the proposed integrated antenna switch architecture. In section 3, the measurement Test Element Groups (TEGs) are explained along with the measurement results. Finally, section 4 concludes the paper. Different than [9], in here, more explanations and analysis about the proposed TRX switch design is explained in detail. More simulations are included about isolation from TX to RX. Moreover, additional measurement structures and results are included in this letter.
2 Proposed integrated antenna switch

The concept is illustrated in Fig. 1(a). In the proposed case, matching blocks of LNA input and PA output are designed along with the considerations of switching transistors’ impedance values when they are biased differently for TX and RX modes. The impedance values for the switching transistors are given in Fig. 1(b) and explained in detail below. The switching biases are different than most transmit/receive switches [3, 4, 5, 6, 7, 8, 9, 10, 11]. In these conventional switches, the switching transistors are biased either at 0 or 1 V. For the proposed work, in TX mode, the PA transistor gate biases are set to 0.7 V considering gain and linearity of TX whereas the LNA gate biases are 0 V. For both LNA and PA transistors drain voltage is 1 V either for ON or OFF cases. The size of the PA transistor is selected as 120 µm total width (2 µm × 60) for higher saturated output power and linearity. In RX mode, the LNA transistor gate biases are set to 0.55 V considering NF of RX whereas the PA gate biases are 0 V. Again, for both LNA and PA transistors drain voltage is 1 V either for ON or OFF cases. The size of the LNA transistor is selected
as 36 µm total width (1.5 µm × 24) for lower NF and gain. Fig. 1(b) represents the impedance seen from the gate of the first-stage transistor of LNA when the biases are 0.55 V for RX mode and 0 V for TX mode. Furthermore, the impedance seen from the drain of the last-stage transistor of PA when biases are 0 V for RX mode and 0.7 V for TX mode. Note that the ON/OFF impedance difference for LNA case is much higher than that of PA. Because of this reason and the importance of RX gain, and NF; the design of LNA input matching block has the priority.

Considering both the ON and OFF impedances of LNA first-stage transistor, a matching block design is presented in Fig. 2(a). In the same figure the impedances at 60 GHz are indicated. Moreover, design is illustrated based on simulations on Smith Chart in Fig. 2(c). The impedance at the gate of the transistor are indicated as \( Z_{\text{LNA,ON}} \) and \( Z_{\text{LNA,OFF}} \). A 150 fF DC cut capacitor is placed before the gate of the transistor for bias and a 115 µm TL is placed. The impedance seen from this point is indicated as ① before the shunt short-circuited TL. A 157.5 µm short-circuited stub is used to match the ON state impedance to 50Ω and that impedance is indicated as ②. With the same stub, the OFF state impedance become inductive. However, in this case the ON/OFF ratio is not high as desired. Hence, another series 115 µm TL is placed. By this way, the ON state impedance still near 50Ω whereas the OFF state impedance become higher than the previous case. The LNA input impedance labels are \( Z_{\text{LNA-IN,ON}} \) and \( Z_{\text{LNA-IN,OFF}} \). Inductive load is required for the OFF state impedance because when PA and LNA are combined the parasitic capacitance of the pad (27 fF) has to be accounted.

Fig. 2(b) presents the PA output matching block design. Similarly, the impedance transformations at 60 GHz are illustrated in the same figure. Moreover, the impedance transformations for the PA design is shown on Smith Chart in Fig. 2(d). Since the ON/OFF impedances seen from the drain side of the last-stage transistor of PA are very close, higher ON/OFF ratio is more difficult to design as compared to LNA case. The impedance at the drain of the transistor are indicated as \( Z_{\text{PA,ON}} \) and \( Z_{\text{PA,OFF}} \). A load connected to VDD is used right after the drain and these impedances are labelled as \( Z_{\text{PA1,ON}} \) and \( Z_{\text{PA1,OFF}} \). In order to block the DC flowing through the LNA and avoid VDD-GND short circuiting a 150 fF of DC cut capacitor is used before the antenna port. To match the impedances after the load and before the DC cut capacitor, a 170 µm open-circuited stub is used after a 170 µm series TL. These points are indicated as ② and ③ in the schematic. Both LNA output port and PA input port are matched to 50Ω.

The PA and LNA are combined directly to a Tee-junction before the antenna port pad. The RX mode of the combined circuitry is shown in Fig. 3(a). Thanks to the high impedance of the PA when it is in OFF state, the loss to TX is calculated to be -1.31 dB at 60 GHz. The antenna input impedance is very close to 50Ω with very small reactive component. Hence, the loss due to reflection in RX mode of the antenna switch circuit is as small as -0.07 dB. As a result, total loss in RX mode from antenna input to LNA input is -1.38 dB. Similarly, the TX mode of the circuitry is shown in Fig. 3(b). In this case, the ON state impedance is close to OFF state and hence it is not well matched to 50Ω mostly due to the required DC cut capacitor. The loss to RX from the PA (TX) output is calculated to be -1.91 dB at 60 GHz due to the mentioned impedance mismatch. The antenna input impedance
in this case is not close to 50 Ω mostly due to the large reactive component (j33 Ω). Hence, the loss due to reflection in TX mode of the antenna switch circuit is around −0.46 dB. As a result, total loss in TX mode from PA output to antenna input is −2.37 dB.

One of the important points to be cleared out is the isolation from PA to LNA, as indicated in Fig. 3(b). The coupled power to the first-stage LNA transistor gate from the PA may open and close the transistor if the voltage amplitude of the coupled power exceeds the transistor threshold voltage value (around 0.4 V in this process) when the output power is large and the isolation is not enough. The peak voltage amplitude versus the output power from PA is calculated for different isolation values and plotted in Fig. 4. For instance, for a TX output power of 3 dBm an isolation of 10 dB is enough to preserve linearity of the TX mode. A conceptual design is made for a two-stage LNA and a two-stage PA. The schematic of the antenna switch circuitry is shown in Fig. 5. The isolation from the last-stage
transistor output of PA to the first-stage transistor input of LNA is simulated and presented in Fig. 6(a). The simulated isolation is less than $-10$ dB in the band of interest. This much isolation is enough for moderate power applications. Moreover, time domain simulation is made for TX output power of 1.6 dBm (simulated OP1dB point) and illustrated in Fig. 6(b). The antenna output time domain signal is illustrated in black and has a maximum of around 0.4 V, and the coupled time domain signal to the gate of LNA transistor is shown in red color which has a peak value of around 0.3 V ($V_{th} = 0.4$ V). The LNA transistor output time domain signal is plotted in blue. One can observe that the peak is less than the input as expected. The design satisfies the requirement for the isolation.
3 Measurement structures and results

LNA only and PA only Test Element Groups (TEGs) are implemented for comparison purposes. However, LNA input pad and PA output pad are just added for measurements. After the measurements these pads are de-embedded for fair comparison since the design of PA and LNA does not include those pads, and the impedances of LNA and PA are designed considering the antenna port pad parasitic capacitance. All TEGs are implemented in 65 nm bulk CMOS process. The overall designed antenna switch (schematic presented in Fig. 5) chip photo is shown in Fig. 7(a). The total area with pads is \(0.78 \times 0.68 \text{ mm}^2\), the core circuit area without pads and DC decoupling capacitors is \(0.42 \times 0.55 \text{ mm}^2 = 0.23 \text{ mm}^2\). Left hand side has a ground-signal-ground (GSG) pad as the antenna port. On the right hand side, a GSGSG pad is used. Upper signal pad is for the output of LNA and lower signal pad is for the input of PA. LNA only TEG chip photo is shown in Fig. 7(b) and the core circuit area without pads and DC decoupling capacitors is \(0.25 \times 0.57 \text{ mm}^2 = 0.143 \text{ mm}^2\), and PA only TEG chip photo is shown in Fig. 7(c) and the core circuit area without pads and DC decoupling capacitors is \(0.23 \times 0.55 \text{ mm}^2 = 0.127 \text{ mm}^2\). The total core area consumption for LNA only and PA only TEGs is calculated to be \(0.27 \text{ mm}^2\). On the other hand, the total core area of the whole system is \(0.23 \text{ mm}^2\). In this work, the area is saved by \(0.04 \text{ mm}^2\). This clears the area advantage. First of all, all circuits are measured with a Vector Network Analyzer (VNA).

Fig. 8(a) presents the antenna port reflection S-Parameter in RX mode for the switch circuit (red line) in comparison with LNA only TEG input port reflection S-Parameter (blue line) from 57 to 66 GHz. As it can be observed when the LNA and PA is combined in considerations with antenna port pad parasitic capacitance, the impedance is close to \(50 \Omega\) point on Smith Chart. Similarly, Fig. 8(b) presents the antenna port reflection S-Parameter in TX mode for the switch circuit (red line) in comparison with PA only TEG input port reflection S-Parameter (blue line) from 57 to 66 GHz. PA only TEG return loss results are more far from the center of Smith Chart when compared to the combined circuits return loss results. From the perspective of matching on the antenna port of the switch circuit, one can say that both TX mode and RX mode are well matched.

The measured gain of LNA (RX, PA is OFF) mode of antenna switch circuit (red line) and de-embedded LNA only circuit (blue line) are presented in Fig. 9(a).
The results are presented from 57 to 66 GHz. TRX switch LNA mode gain is around 10 dB at 60 GHz. The gain difference between the TRX switch LNA mode and the LNA only is between 1.1 to 1.7 dB. The minimum value is much smaller than one can achieve with a conventional switch structure. The NF of TRX switch and LNA only TEG is measured and presented in Fig. 9(b). The red dots are the NF of TRX switch RX mode and the blue dots are the NF of LNA only TEG.
Moreover, black dots represents the NF degradation due to the LNA and PA combination of antenna switch circuitry. The NF degradation aligns with the gain degradation of LNA circuit. The NF of RX mode is measured to be 2.9 dB at lowest. LNA only TEG has a NF as low as 1.9 dB.

The measured gain of PA (TX, LNA is OFF) mode of antenna switch circuit (red line) and de-embedded PA only circuit (blue line) are presented in Fig. 10(a) from 57 to 67 GHz. TRX switch PA mode gain has a maximum of around 12 dB at 65 GHz. PA only measured gain has a maximum of around 14 dB around 65 GHz. The gain difference between the TRX switch PA mode and the PA only is between 2.3 to 2.7 dB. The difference is flat which is desired for a wideband system gain flatness. However, the introduced loss is higher than the LNA case. As explained in the previous section, it is mostly because of matching the PA for ON state to 50Ω.

The main loss contribution is from the reflection and impedance mismatch between OFF state LNA and ON state PA. Fig. 10(b) presents the input-output power relation when only PA in blue line and PA mode of switch circuit in red line.

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lower than the introduced loss by the TRX switch combination which is around $-2.3\,\text{dB}$. Moreover, one can understand the isolation is not an issue at this $\text{OP}_{1\text{dB}}$ since the degradation of linearity is lower than the combined switch loss.

### 4 Conclusions

Table I presents the comparison table of the proposed structure with other state-of-the-art switch circuits. Proposed antenna switch has a loss in RX mode as low as $1.1\,\text{dB}$ which is the lowest presented in the table. Hence, the NF degradation for RX is the lowest in the presented mode. The minimum NF for this work is measured as $2.9\,\text{dB}$. Another clear advantage of the proposed work is the silicon area consumption, since the design does not use any additional switch or transmission lines. As indicated, matching blocks are re-used for switching purposes in consideration with the switch as re-using the transistor of last-stage of PA and first-stage of LNA. For massive MIMO applications or phased array applications, this method helps to save considerable silicon area. The loss in TX mode is higher than expected. One reason is the modeling issue of transistors. By using more accurate models, much lower loss is possible without degradation of TX linearity or gain.

Both PA and LNA ON and OFF impedances are carefully designed to achieve this low loss antenna switching circuit. The presented switch method has several advantages in terms of area, lower loss, and lower NF degradation. The simulated isolation value of $-14\,\text{dB}$ shows that the switch can work properly at an output power of $\text{OP}_{1\text{dB}} = 2\,\text{dBm}$, without any degradation on the linearity other than introduced loss of the switching architecture.

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