LETTER

A 24-bit sigma-delta ADC with configurable chopping scheme

Li Li¹, Xu Cheng^{1a)}, Zhang Zhang², Jianmin Zeng², and Xiaoyang Zeng^{1b)}

Abstract This paper presents a low-power high-precision sigma-delta analog-to-digital converter (ADC) mainly used for DC measurement, especially in applications with high input impedance. A configurable chopping scheme is proposed to reduce the input-dependent residual offset caused by the clock feed-through. Furthermore, it also improves noise performance in the first integrator. The 1.17 mm² chip is fabricated in a standard 65 nm CMOS process. Measurement results show that the ADC achieves 20-bit resolution, 10 ppm INL and a 0.6 μV offset, while consuming 860 μW from 3.3 V supply.

Keywords: delta-sigma modulator, analog-to-digital converter, low-voltage low-power analog circuit

Classification: Integrated circuits

1. Introduction

The scaling down of CMOS technology continuously pushes digital systems to have higher density, higher speed, and lower cost. The technology scaling is generally associated with a decrease in supply voltage, which reduces the signal swing and circuit dynamic range [1]. This trend brings great difficulties to the design of a high resolution analog-to-digital converter (ADC). Meanwhile, low power consumption becomes more critical in modern integrated circuit design to meet the increasing demands of the battery-powered portable device [2]. Sigma-delta ADCs are widely used in the low-power and low-frequency applications [3, 4, 5, 6, 7, 8, 9, 10].

As for DC measurement applications, noise and offset are the biggest issues, and chopper stabilization technique has been widely used in the design of the modulator [11, 12, 13, 14]. But it is difficult to achieve a high noise performance by using the conventional chopping scheme [15, 16], due to the residual offset and the noise in the first integrator. In order to solve these problems, this paper proposes a configurable chopping scheme including an adjustable delay cell between choppers, an additional pair of choppers to reduce the noise in the integrator, as well as a double gain mode to amplify especial small input. For residual offset, there are several techniques that can be used to alleviate this problem caused by clock feed-through

spikes, such as Nested-chopper technique [17] and chopper with guard band [18, 19]. But Nested-chopper technique needs an additional sequential logic and complicates the design of a switch-capacitor system, and the chopper with guard time must generate a large delay to endure the variation of input impedance. The method by adding a configurable delay in this paper has been proved to be efficient by the simulation and test results.

This paper is organized as follows, Section 2 describes the architecture of the modulator, Section 3 introduces the proposed chopping strategy, the measurement results are presented in Section 4, and the conclusion is given in the last section.

2. Architecture of the proposed ADC

The architecture of the modulator in Z-domain is depicted in Fig. 1. The feed-forward architecture is chosen as the noise-shape topology of the proposed design for its low-distortion characteristic [20], in addition, the single-bit quantizer is adopted to avoid design complexities [21, 22]. In order to achieve more than 120 dB SNR at DC input signals a third-order noise shaping is used. The transfer function of the sigma-delta modulator is given by [23, 24, 25]:

$$V(z) = STF(z)U(z) + NTF(z)E(z), \quad (1)$$

where NTF(z) is the noise transfer function of the modulator in z domain, STF(z) is the signal transfer function. By using the behaviors model simulations in MATLAB, the coefficient of each integrator is determined to prevent overload of the output of the ADC. The gain coefficients of each block are set to:

$$\begin{aligned} a_1 = 10/34, \quad a_2 = 11/34, \quad a_3 = 5/34, \quad b_1 = 1/3, \\ b_2 = b_3 = b_4 = 0, \quad c_1 = c_2 = c_3 = 1/5 \end{aligned} \quad (2)$$

Fig. 1. Architecture of the modulator in Z-domain.

¹State Key Laboratory of ASIC and System, Fudan University, Shanghai 201203, China

²School of Electronic Science and Applied Physics, Hefei University of Technology, 193 tunxi Rd. Hefei, 230009, China

a) chengxu@fudan.edu.cn

b) xyzeng@fudan.edu.cn

Fig. 2. Block diagram of the proposed ADC.

Fig. 2 shows the block diagram of the proposed sigma-delta ADC. The supply voltage of the decimation filter and the logic control block in the modulator is set to a minimum of 1.0 V to reduce the power consumption. Meanwhile, to make the system have a relatively large dynamic range, the analog circuitry in the modulator operates at 1.8 to 3.3 V by employing the IO MOSFETs. Besides, the signal path for interaction between the two voltage domains needs a corresponding level shifter inserted for signal level conversion. The level shifter from the high voltage domain to the low voltage domain is shown in the Fig. 2, as well as the one from the low voltage domain to the high voltage domain. When ADC is used in high-precision measurement applications, the analog supply voltage is set to 3.3 V to obtain the maximum dynamic range, and the supply voltage is reduced to 1.8 V to further reduce the overall power consumption in medium-accuracy applications.

3. Proposed configurable chopping scheme

Fig. 3. Clock feed-through model in a chopper.

For a traditional chopper block [26, 27] shown in Fig. 3, the residual offset (V_{OS}) is mainly caused by the demodulated current spikes and mismatch of the signal path. At the transition moments of the chopper clocks, due to clock feed-through the mismatch between the capacitances causes an AC current spike. This AC current spike is rectified by M_1 , which appears as a DC spike current at the input of M_1 . The average value of DC spike current at the input of M_1 is given by:

$$I_{offset} = 2(\Delta C_1 - \Delta C_2)V_{clk}f_{CH}, \quad (3)$$

where ΔC_1 and ΔC_2 are the mismatch parasitic capacitance in the chopper, V_{clk} is the amplitude of the clock signal, and f_{CH} is the frequency of the chopping clock. This current goes through the series impedance of the chopper and the input signal source, leading to an input voltage spike. The average DC value of the spike results in a residual offset V_{OS} , as given by:

$$V_{OS} = 2R(\Delta C_1 - \Delta C_2)V_{clk}f_{CH}, \quad (4)$$

where R is the input impedance including the impedance of the signal source and the on-resistance of the chopper switch. The average DC value of the spike results in a residual offset. This spike voltage also causes low-frequency interference and can be cancelled out by adding a proper delay between the two choppers. Since the time constant varies with the source impedance, the delay should be adjustable when the input impedance is changing, especially in a reconfigurable system. The proposed configurable chopper technique is shown in Fig. 4.

Fig. 4. Delay strategy of the chopper stabilization.

M_1 and M_2 are the choppers in the first integrator, while $m_1(t)$ and $m_2(t)$ are the chopper clock signals respectively. When the input signal is modulated by M_1 , there is a chopping spike caused by clock feed-through, which generates the residual offset. If the signal is demodulated with a clock properly delayed, such spikes are cancelled out by the positive and negative components. In order to obtain a configurable delay, an inverter chain is set to generate the required delay between the choppers, and this delay can be controlled by changing the number of inverters in the chain, which makes the signal always demodulated at the midpoint of the spike. As a result, the residual offset is compensated and the average output dc voltage of M_2 is around zero. When a signal source with higher impedance is used as the input of the system, the time constant τ of the spike voltage increases accordingly, and at this time the configurable delay increases by adding the number of the inverters in the delay chain.

In such a 3rd-order modulator system a residual offset less than 10 μ V cannot be achieved by using the single chopper stabilization to the amplifier, because the mismatch in the external signal path of the amplifier also deteriorates the performance. Hence two independent set of chopper switches are adopted in the system. The input

Fig. 5. Circuit implementation of the modulator.

signal is modulated by non-overlapping clocks (CLK_{CHA2} and CLK_{CHB2}) at the sampling terminal with one chopper, and it is demodulated at the input of the second integrator. Therefore, the low-frequency interference of the first integrator generated by the mismatch is modulated to the chopping frequency, away from the baseband. The other chopper (M_1 and M_2) is employed between the input and output terminal of the amplifier to attenuate the offset and noise of the amplifier, and this chopper is controlled by the clock signals CLK_{CHA} and CLK_{CHB} . The circuit implementation is shown in Fig. 5. The specific sampling strategy with chopper stabilization is as follows: a pair of reference voltages, i.e. V_{refp} and V_{refn} of the system are sampled by the feedback capacitor C_F under the joint action of clock phases ϕ_1 and ϕ_2 as well as the feedback signal, then the sampling signal is used as the input of the chopper M_1 , while the input signal of the first integrator is sampled by the capacitor C_{S1} under the control of clock signal CLK_{1d_cha} and CLK_{1d_chb} which are generated by chopping clock signals and sampling clock signals through the NAND gate.

As mentioned in Section 2, to collect signals with small amplitude, the modulator adopts two gain modes, i.e. unity gain and double gain. The overall gain of the modulator is changed mainly by configuring the gain for the first integrator. When configured to be in the high gain mode, an additional input signal and an additional sampling capacitor are added to the sampling path of integrator. At this time, the clock phase $\phi_{1d_g_cha}$ is exactly the same as the clock phase ϕ_{1d_cha} . Furthermore, the three pairs of clock phases, i.e. ϕ_{2d_g} and ϕ_{2d} , ϕ_{2_g} and ϕ_2 as well as ϕ_{1_g} and ϕ_1 are also consistent. It is equivalent to that the sampling capacitor at the signal input terminal C_{S1} is doubled, thus achieving the effect of doubled gain. When the high gain mode of the circuit is turned off, the switches

for the additional sampling path are all turned off, and the modulator operates in the unity gain mode.

4. Modeling of residual offset and simulation results

We simplify the offset caused by clock feed-through as a spike voltage discharge through a capacitor, the residual offset at the input of chopper M_1 can be calculated as:

$$V_{os} = 2f_{CH} V_{spike} \tau, \quad (5)$$

where the time constant τ of the spike voltage is the product of the input impedance R and mismatch parasitic capacitance in the chopper. When a delay t is introduced between the two choppers, the average of residual offset is given by:

$$V_{os_ave} = 2f_{CH} \left| \int_0^t V_{spike} e^{-x/\tau} dx - \int_t^\infty V_{spike} e^{-x/\tau} dx \right|. \quad (6)$$

Fig. 6 shows the relationship between residual offset and delay, the empirical value of the optimal delay is 70% of the time constant according to the simulation.

Fig. 6. Relationship between delay time and residual offset.

Fig. 7. Simulation results of the proposed chopping scheme.

In order to verify the proposed chopping scheme, the proposed ADC is simulated with 100 k Ω input impedance. As shown in Fig. 7, the ADC achieves the peak SNR of 127.7 dB, 132.3 dB, and 134.8 dB when three schemes employing no chopping, the conventional chopping, and the proposed chopping, respectively. Also the simulation reveals the relationship between delay in chopper and SNR, and there is a 1 dB improvement when an appropriate value is chosen.

Fig. 8. Chip micrograph.

5. Implementation and experimental results

The proposed sigma-delta ADC has been implemented in a 65 nm standard CMOS process. Fig. 8 shows the die photograph with a core area of 1.17 mm^2 .

Fig. 9 shows the output spectrum of the sigma-delta modulator, where a 454 Hz -4 dBFS sinusoidal input is introduced, and the noise floor at low frequency is about 125 dB. Fig. 10 gives the histogram of 1000 repeated measures with shorted inputs. The average value of the offset is $0.6 \mu\text{V}$ (3LSB). Typical measurement results are shown in Fig. 11 for the output noise, in a conversion time of 10 ms, an output noise of $0.741 \mu\text{V}_{\text{RMS}}$ is measured with a 40 KHz chopping frequency. The maximum SNR at DC can be obtained by (7), resulting in a value of 124 dB.

$$SNR_{\text{max}} = 20 \cdot \log((\max DCinput / 2\sqrt{2}) / \text{noise}), \quad (7)$$

The maximum SNR at DC deteriorates to 117.4 dB when the choppers are shut down. The range of the delay is between 20 ns and 400 ns, the optimal value of delay is too small to find under the test environment with very small input impedance. Fig. 12 shows that the performance of SNR_{MAX} can be improved by 0.17 dB by changing the delay within the set range. As illustrated in Fig. 13, the ADC's linearity is limited by mismatch, resulting in an INL performance of about $\pm 10 \text{ ppm}$. The offset of the chip at different temperature is shown in Fig. 14 with the range from -40 to 80°C . The maximum offset of the chip is $3.1 \mu\text{V}$. The measured power consumption of the analog circuit is $760 \mu\text{W}$ at a supply voltage of 3.3 V , and the digital decimation filter consumes $100 \mu\text{A}$ currents under 1 V . Table I compares this work with other state-of-the-art high resolution ADCs [28, 29, 30]. The figure-of-merit (FOM) can be calculated as follow [20]:

$$FoM = SNR_{\text{MAX}} + 10 \log\left(\frac{1}{\text{Power} \cdot 2T}\right), \quad (8)$$

in which T is the conversion time, and SNR is the measured maximum SNR. The formula enables a fair comparison with ADCs characterized by using a sine input. This work achieves a FoM of 172 dB which indicates a favorable low-power and high-precision achievement.

Fig. 9. Measured output spectrum of the modulator with 454 Hz sinusoidal signal.

Fig. 10. Histogram distribution of measured offset.

Fig. 11. Measured output noise versus DC voltage.

Fig. 12. Measured maximum SNR versus delay time.

Fig. 13. Measured integral nonlinearity.

Fig. 14. Measured offset at different temperature.

Table I. Comparison with the state-of-art results

Parameter	[28]	[29]	[30]	This work
Technology	0.6 μm	0.18 μm	0.16 μm	65 nm
Chip area (mm^2)	2.08	2.4	0.375	1.17
Supply voltage (V)	2.7–5.0	3.3	1.8	1.8–3.3
Conversion time (ms)	66.7	0.512	40	10
Measured Noise (μV_{RMS})	2.5	4.13	0.65	0.741
SNR_{MAX} @ DC (dB)	123	110.7	119.8	124
DC offset (μV)	2(typ) 10(max)	1.5(typ)	0.5(typ) 1(max)	0.6(typ) 3.1(max)
INL (ppm)	± 5	-	± 6	± 10
Power consumption (μW)	600	5940	6.3	860
FoM (dB)	166.4	162.8	182.7	172

6. Conclusion

A 24-bit sigma-delta ADC with configurable chopping scheme is proposed. It overcomes the residual offset caused by clock feed-through, as well as the mismatch in the first integrator. A configurable delay cell is employed to reduce the chopping spikes. Meanwhile, an additional chopper is applied to cancel the mismatch of the integrator. Further-

more, a prototype of the proposed ADC is integrated in a 65 nm CMOS technology and achieves a RMS noise of $0.741 \mu\text{V}$. The measurement results reveal a 6.7 dB improvement in SNR_{MAX} with the chopping strategy. This technique is suitable to the DC measurement with high input impedance.

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