LETTER

An architecture design for anti-jamming circuit with low power and low area cost in high-precision GNSS receiver chip

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Abstract In this paper we propose an architecture of the anti-jamming circuit in high precision GNSS receiver chip base on the frequency-time domain solution, at most, the jamming signals of 12 frequency points can be detected and eliminated at the same time. In addition, an jamming detection strategy based on short-long time FFT is proposed and a circuit of FFT engine with low cost is designed to reduce the area and dynamic power of the GNSS receiver chip. Finally, we complete the VLSI design by using 55 nm digital process, the circuit area is 0.082 mm², the average dynamic power is 0.943 mW. The implementation results prove the effectiveness of the proposed anti-jamming circuit.

Keywords: GNSS receiver, anti-jamming, VLSI, FFT engine

Classification: Integrated circuits

1. Introduction

Global Navigation Satellite System (GNSS) can effectively resist narrowband jamming by using direct spread spectrum sequence signals. However, when the energy of the jamming source exceeds the anti-jamming ability of the system, the performance of the GNSS receiver will be seriously degraded [1, 2]. Therefore, additional anti-jamming technology is necessary to improve the anti-jamming ability of the GNSS receiver.

Recently, many anti-jamming technology of GNSS receiver mainly focuses on the space, frequency, time domain solution [3, 4]. Additional antenna arrays that are assembled at specific locations are needed in the space domain solution to resolve the jamming issues [5, 6, 7, 8], and the estimation of jamming frequency depends on the parameters of ADC in each antenna. However, in practice, the parameters of ADCs in multi-antenna are different, which makes it difficult to estimate the jamming frequencies accurately [9]. The space domain solution will also increase the cost of the GNSS receiver system significantly. The frequency domain solution detects the frequency of jamming by Fast Fourier Transform (FFT), and recovers the GNSS signals by Inverse Fast Fourier Transform (IFFT) after the jamming frequencies are removed [10, 11, 12, 13]. The advantage of frequency domain solution

is that multiple jamming signals can be detected and eliminated in parallel, the solution has an extremely high efficiency to suppress the jamming signals. However, its disadvantages are also obvious for VLSI design [14, 15], which requires high area cost and dynamic power for the FFT and IFFT circuit. The time domain solution mainly utilizes the correlation of narrowband jamming to predict the frequency of the jamming signals in the current signal, and uses the adaptive notch filter (ANF) to suppress the jamming signals [16, 17, 18, 19, 20]. Although the hardware resources of the time domain solution have the lowest requirements compared with other solutions, if there are multiple jamming signals in the GNSS signal, the jamming signals can only be detected and eliminated serially. And due to the time domain solution must work at the sampling clock domain of the RF ADC, the jamming detection circuit has less efficient for circuit implementation. In addition to the above anti-jamming solutions, other auxiliary solutions have been proposed in recent years. An anti-jamming solution based on Assisted GNSS (A-GNSS) has been proposed in [21]. And the Inertial Navigation System (INS) is used to improve the anti-jamming ability of GNSS receivers in [22, 23]. But these solutions require additional information of base station or INS equipment.

In order to achieve high performance of positioning, the high-precision GNSS receivers need to support multi-frequency GNSS signals, each frequency point of GNSS signal requires an independent anti-jamming circuit, and the anti-jamming circuit needs to be turned on continuously to ensure the continuity of the GNSS signals.

According to the requirements of real-time, area and dynamic power of the high-precision GNSS receiver chip, we propose an architecture of anti-jamming circuit base on frequency-time domain. The frequency domain solution is used to detect the jamming signals by FFT only, and the cascading filters in time domain are used to eliminate the jamming signals. The proposed solution significantly reduces the area and dynamic power of the circuit compared with traditional frequency domain solutions. And we propose a jamming detection strategy based on short-long time FFT, which allows short-time FFT with less computational complexity to be used in the jamming detection phase to reduce the average dynamic power of the circuit. And according to the strategy, the circuit of a configurable FFT engine is designed, which can support up to 1024-point FFT, the address control logic of the FFT engine is optimized, reducing the area of RAM by about 50% compared with other structures. In addition, an adaptive

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data width limiting circuit is proposed to effectively reduce the data width of the RAM circuit without loss of jamming detection performance. Compared with other structures, the FFT engine designed in this paper can reduce the area of RAM by about 75% and the dynamic power by about 60% under the same conditions of jamming detection accuracy and the detection period.

The rest of this paper is organized as follows. In Section 2, we introduce the architecture of proposed anti-jamming circuit. Focusing on the area cost and dynamic power of the circuit in jamming detect phase, an FFT engine is proposed in Section 3. And the experimental results of the circuit and the comparisons with other papers are presented in Section 4, which is followed by the conclusion in Section 5.

2. Proposed architecture of anti-jamming circuit

2.1 Traditional architecture of frequency domain

Since the high efficiency of jamming detection in frequency solution, high-precision GNSS receivers usually use frequency-domain solution to cope with the application scenarios which exist multi-frequency jamming or the jamming frequency changing rapidly. The GNSS signal with multi-frequency jamming is shown as Eq. (1), where $s(t)$ is the GNSS signal, $n(t)$ is the white Gaussian noise, K is the amount of the jamming signals, A_k, f_k are the amplitude and the frequency of the jamming signals respectively.

$$x(t) = s(t) + n(t) + \sum_{k=1}^K A_k \cos(2\pi f_k t) \quad (1)$$

The frequency-domain anti-jamming solution needs to perform FFT operation on the input signal firstly, the input GNSS signal is continuous, it means that the input signal is truncated in batches by FFT operation, FFT implies the periodic extension on the input signal. When the truncated input signal is extended periodically, it is not continuous at the truncated edge. It will cause spectrum leakage, which will seriously affect the accuracy of jamming frequency estimation. The usual processing method is adding windows on the input signal, so that the truncated input signal becomes smoother along the edge after periodic extension, but the distortion of the input signal will be caused by the windowing operation.

The traditional frequency domain solution adopts overlapping windows method to reduce signal distortion. As shown in Fig. 1, the traditional solution uses two branches to detect jamming frequencies by FFT, and recover the signal from frequency domain to time domain by IFFT to compensate for the loss of GNSS signal caused by windowing operation in each branch.

Fig. 1. The traditional architecture of frequency-domain

As shown in Fig. 1, two independent groups of FFT and IFFT operations are required in traditional frequency domain solution. For the GNSS receiver chips, the solution requires a large scale of hardware resources to implement the FFT and IFFT operation. Moreover, in order to ensure the continuity of the output IF signal, the IF signal recovered by the IFFT circuit should be consistent with the output frequency of the ADC of RF front-end, hence, the IFFT circuit usually work at a higher clock frequency, which will improve the dynamic power of the circuit significantly. Especially when the solution improves the operation points of FFT to improve the detection accuracy of jamming frequency, the area cost and dynamic power of the GNSS receiver chips will be unacceptable. But if the operation points of FFT are reduced, the detection accuracy of the jamming frequency will also be reduced.

2.2 Proposed architecture

In order to overcome the shortcomings of the traditional anti-jamming solution in frequency domain, as well as reducing the area cost and dynamic power of the GNSS receiver chip, in this paper, an architecture of anti-jamming circuit in frequency-time domain is proposed, which only performs frequency point detection of jamming signals in the frequency domain, and suppresses the jamming signals by the configurable cascade time-domain filter. The proposed architecture of anti-jamming circuit in this paper and the connection with other circuits in the GNSS receiver chip are shown in Fig. 2.

The circuit architecture in Fig. 2 mainly consists of a jamming frequencies detection circuit in frequency-domain and a configurable cascade notch filter in time-domain. The clock frequency of the cascade notch filter is same as the output frequency of the ADC in RF front-end, and the jamming detection circuit works at the high performance clock domain of 200 MHz. The jamming detection circuit is the key part of the architecture and the main contribution of this paper. It includes a windowing circuit, a configurable FFT engine, a spectrum selection circuit, a noise statistics circuit, and a jamming decision circuit.

Fig. 2. The proposed architecture of anti-jamming circuit

As shown in Fig. 2, the cascade time-domain notch filter adopts the structure of second-order IIR filter with smaller area cost, it consists of 12 stages notch filter. The parameters of each notch filter can be configured by the

HOST MCU in the GNSS receiver chip flexibly. The operation points of the configurable FFT engine in the jamming detection circuit can also be configured by the HOST MCU, and up to 1024 points of FFT operation can be realized.

In addition, the jamming decision circuit in Fig. 2 adopts an adaptive threshold of the first-order distance solution to detect the frequency of the jamming signals. The threshold A_{th} for decision the amplitude of jamming signals is shown as Eq. (2), where N is the number of spectrum lines in FFT results, a_j is the amplitude of one of the spectrum lines, λ is the scaling factor of the threshold, the general value of λ is between 3 and 5. In this paper $\lambda = 5$, any spectral line whose the amplitude exceeds A_{th} is considered as a jamming signal.

$$A_{th} = \lambda \frac{1}{N} \sum_{j=1}^N a_j \quad (2)$$

In Fig. 2, A_{th} is calculated by the noise statistical circuit, Eq. (2) shows that A_{th} is only related to the statistical characteristics of the amplitude of the spectrum lines, but not sensitive to the specific amplitude of the spectrum lines. Moreover, when FFT engine with lower points is used, the solution can still detect the frequency of the jamming signals roughly.

The work flow of the anti-jamming architecture proposed in this paper can be briefly described as follows:

(1) In the initialization stage, the cascade notch filter is in full pass state. The frequency spectrum lines of GNSS signal are obtained by short-time FFT operation (256 points) by the FFT engine after adding window. Then the current amplitude of spectrum lines and the value of threshold are roughly judged by the jamming decision circuit. And the decision results of current stage are read and recorded by the HOST MCU.

(2) After step (1), when the jamming signals are detected by the HOST MCU, the FFT engine is configured to perform a long-term FFT operation (1024 points) and repeat the operation in step (1). As the operation points of the FFT engine increase, the frequency point of the jamming signals can be estimated accurately.

(3) After step (2), HOST MCU calculates and configures the working parameters of all notch filters according to the accurately frequency point of the detected jamming signals, in order to eliminate the jamming signals of each frequency in parallel.

(4) After the above operations, 12 different frequencies of jamming signals can be eliminated in current GNSS signal at most. Meanwhile, the FFT engine is reconfigured by HOST MCU to perform the short-time FFT operation to continuously monitor the changes of jamming signals, in order to maintain a lower dynamic power. When the frequency changes of the current jamming signals are detected by the HOST MCU, which stores the current results and repeats the operations from step (2) to step (4).

Since the architecture of the anti-jamming circuit proposed in this paper directly eliminated the jamming signals in time-domain solution, the IFFT operation is not required compared with the traditional architecture of frequency-

domain. Moreover, the redundant circuit structure of the upper and lower branches of the overlapped window is not required in this paper to compensate for the loss of the amplitude of the input signal caused by windowing. Only one FFT engine is used in the overall architecture, and the FFT calculation is only 25% of the traditional architecture, while retaining the advantages of high efficiency of jamming detection in frequency-domain solution, the dynamic power and area cost of the GNSS receiver chip are reduced observably. On the other hand, since the jamming detection solution of the short-long time FFT is proposed in this paper, compared with other published works, the GNSS receiver chip has lower average dynamic power in the jamming detection phase without losing the accuracy.

3. Proposed configurable FFT engine

3.1 Traditional structure of FFT engine

Compared with the traditional architecture of anti-jamming circuit in frequency-domain solution, the proposed architecture has obvious advantages in the area cost and dynamic power of the circuit. However, the high-precision GNSS receivers need to support multi-frequency GNSS signals, and an independent anti-jamming circuit is required by each frequency GNSS signal. Therefore, we still hope to further reduce the area cost and the dynamic power of the anti-jamming circuit.

Considering the above factors, the FFT engine designed in this paper adopts a serial structure, which contains only one radix-2 butterfly unit (BU) to minimize the area and dynamic power of the circuit. The traditional serial structure of FFT engine is shown in Fig. 3 [11, 12].

Fig. 3. The traditional serial structure of FFT engine

Assuming that the data length of the FFT is N , the FFT engine requires a total of $m = \log_2 N$ stages operations, and $N/2$ butterfly calculations (BC) are performed for each stage of operation. But the single-port RAM can not perform read and write operation in one clock cycle, Therefore, the FFT engine in Fig. 3 adopts the structure of ping-pong RAM, and the ping-pong operation between stages ensures the efficiency of the FFT engine, which means that the FFT engine requires redundant area cost of RAM.

3.2 Proposed FFT engine

Although the traditional FFT engine can ensure the efficiency of operation, when the operation points of FFT is increasing, the area and power of the RAM will become an indispensable factor in the GNSS receiver chip. Dual-port

RAM is used in [10] to reduce circuit area, but compared with single-port RAM, it still has larger area and power.

In order to reduce the redundant area of RAM, the address controller of RAM in FFT engine is optimized in this paper. The address order read by BU can be expressed by Eq. (3), Eq. (4) and Eq. (5), where $p(k, n)$ and $q(k, n)$ are the input data of BU, A is the addresses of $p(k, n)$ or $q(k, n)$ in RAM, k is the current operation stage, n is the order of calculation in each stage, and N is the data length.

$$A_{p(k,n)} = \begin{cases} j_n, & n \bmod 2 = 0 \\ j_n + N/2, & n \bmod 2 = 1 \end{cases} \quad (3)$$

$$A_{q(k,n)} = \begin{cases} j_n + N/2^k, & n \bmod 2 = 0 \\ j_n + N/2^k + N/2, & n \bmod 2 = 1 \end{cases} \quad (4)$$

$$j_n = \begin{cases} 0, & n = 0 \\ 2 \times n, & n \bmod N/2^k = 0 \\ j_{n-1} + 1, & \text{others} \end{cases} \quad (5)$$

Eq. (3) and Eq. (4) show that the distance between the data addresses of the two adjacent calculations is equal to $N/2$. Based on this condition, we divide the input data into two segments and store them in two blocks of RAM, but the area of each RAM is 50% of the RAM in Fig. 3 the same efficiency is achieved, the former $N/2$ data is stored in RAM0, and the latter $N/2$ data is stored in RAM1. It means that the optimized FFT engine can use ping-pong operation at the same calculation stage, when the RAM0 is read by BU, the RAM1 is in an idle state to allow the results of the BU to be written, the area of the RAM is reduced by 50% compared to the traditional structure in Fig. 3 which the ping-pong operation is performed between stages. The FFT engine proposed in this paper is shown in Fig. 4.

Fig. 4. Proposed structure of FFT engine

The adaptive bit-width limiter in Fig. 4 is another contribution of this paper. BU records the maximum value of the results of the current calculation stage, when the next stage of calculation is performed, the maximum value is compared with the threshold value. Since the maximum bit-width of the results of BU is increased by 2-bit each calculation, the value of threshold should be set to 25% of the maximum value in order to ensure that the results of next calculation does not exceed the maximum bit width set by the system. When the maximum value of the previous calculation is detected to exceed the threshold,

all results in current stage are shifted to the right by 2 bits uniformly. The advantage of the circuit is that when the energy of the jamming signal is strong, the bit-width of the BU and the RAM can be effectively limited, and remain the statistical characteristics of the signal spectrum. Fig. 5 and Fig. 6 show the spectrum results of original fixed-point FFT and the proposed FFT engine with single-frequency jamming signal. It can be seen that the proposed FFT engine retains the characteristics of spectrum well, and effectively reduces the magnitude. The magnitudes in Fig. 5 and Fig. 6 are the square roots of the real and imaginary parts of the results.

Fig. 5. Results of original FFT with 12-bit quantized input

Fig. 6. Result of proposed FFT engine with 12-bit quantized input

Taking input data quantized by 12-bit and the length of 1024 points as an example. The maximum bit-width of the FFT engine in this paper is 16-bit, while the traditional structure needs 32-bit to save the temporary results, and by optimizing the address control logic, the redundant RAM in the traditional structure is reduced. Compared with the traditional structure, the area of RAM in FFT engine proposed in this paper can be reduced by about 75%, and the area cost and power of anti-jamming circuit can be further reduced with the same computing efficiency and jamming detection accuracy.

4. Results and comparison

As a part of the high-precision GNSS receiver chip, the anti-jamming circuit proposed in this paper is fabricated in 55 nm digital technology.

Table I shows the results under the conditions of 1.08 V voltage and 125 °C (Worst-Corner). The layout of SoC chip for high-precision GNSS receiver is shown in Fig. 7, which includes the proposed anti-jamming circuit.

Table I. The results of anti-jamming circuit.

Area (mm ²)	Maximum Clock Frequency (MHz)	Peak power (mW)	Average power (mW)
0.0823	204	4.715	0.943

The die size is $6.2 \times 6.4 \text{ mm}^2$ and the measured average dynamic power is about 100 mW. According to the data in Table I, the anti-jamming circuit does not increase the area and dynamic power of the GNSS receiver chip significantly. It achieves the design target of low area cost and low power.

Fig. 7. The layout of the high-precision GNSS receiver

Table II shows the comparison between the proposed architecture of the anti-jamming circuit and other published works. It can be seen that the proposed architecture has obvious advantages in the efficiency and circuit area of jamming detection.

Table II. Comparison of the Architectures of jamming detection circuit (clock frequency 200 MHz, input data quantized by 12 bits).

	Traditional frequency solution [11, 14]	Multiple short-time FFT [12, 15]	Proposed
Operation of butterfly unit	5120	1024	3072
Time of jamming detection (ms)	0.051	0.010	0.015
Number of butterfly units	1	1	1
RAM resources (KByte)	16	4	4
Points of FFT Operation	1024	256	256 and 1024

In order to prove the effectiveness of the anti-jamming circuit intuitively, the circuit is verified by the FPGA prototype of the GNSS receiver chip. 12 frequencies of jamming signals are the input data. After the processing of anti-jamming circuit, the data are sent back to PC through the FPGA for spectrum analysis. The original spectrum and the spectrum processed by anti-jamming circuit are shown in Fig. 8 and Fig. 9. It can be seen that the jamming signals of 12 frequencies can be effectively suppressed by the proposed anti-jamming circuit.

Fig. 8. The original spectrum of 12 jamming signals **Fig. 9.** The spectrum processed by anti-jamming circuit

5. Conclusion

We propose an architecture of anti-jamming circuit in high precision GNSS receiver chip, which adopts frequency-time domain solution, and propose a jamming detection scheme base on long-short-time FFT and the configurable FFT engine circuit is designed. The address logic of the RAM is optimized. Without losing of efficiency, the area of RAM is greatly reduced. And according to the jamming detection algorithm, an adaptive bit-width limiter circuit is proposed, which effectively reduces the data bit-width of circuit and preserves the characteristics of signal spectrum. Compared with other published works, the proposed architecture has low circuit area and dynamic power.

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