LETTER

A low-overhead error detection and correction technique with a relaxed error timing constraint for variation-tolerance

Zhi-jiu Zhu^{1,2a)}, Yi Yu^{1,2}, Xu Bai^{1,2}, Shu-shan Qiao^{1,2b)}, and Yong Hei²

Abstract Variation poses a guard-band requirement for integrated circuit designs, which degrades performance and energy efficiency. As the voltage scales down, the circuits are more sensitive to the variation and the guard-band margin becomes unacceptable. In this paper, we propose a novel error detection and correction technique to eliminate the margin for variation. The error detection latch introduces the low overhead of only 6 transistors compared to the conventional latch. The detection and correction scheme relaxes the timing constraint for the error signal by one clock cycle by extending another latch stage next to the critical stage. The proposed technique reduces the energy per cycle by 51% with 7.6% area overhead compared to the conventional margin technique. Comparison with other works in the state of art shows the proposed technique is quite competitive.

Keywords: adaptive, variation, DVFS, AVS, error detection correction

Classification: Integrated circuits

1. Introduction

The development of the Internet of Things (IoT) [1, 2] has posed stringent requirements for energy-efficient integrated circuits [3, 4]. Among all the low power techniques in circuit level, voltage scaling is considered to be the most effective method due to the quadratic relation between dynamic power and supply voltage [5, 6]. However, voltage scaling aggravates the circuit sensitivity to process, voltage, and temperature (PVT) variations gravely, increasing the risk of timing-margin failure [7, 8]. Therefore, how to operate the circuits robustly in low voltage in the presence of variations is the main focus of ultra-low-power designs.

Variations can be classified into static or dynamic [9]. Static variations exist over the chip lifetime or for an extremely long time, such as process variation or aging effect [10, 11], while dynamic variations affect the chip temporarily, such as voltage droops [12], temperature changes [13], and workload fluctuations. Dynamic variations can be further partitioned to fast-changing or slow-changing according to the time scale of the variations.

In standard voltage designs, worst-case variations are covered by sparing timing margin as a guard band [14]. As the voltage scales down, this method is not feasible due to the unacceptable overhead of the timing margin needed [15].

Adaptive techniques are proposed to minimize the impact of the variation to performance and energy [16, 17, 18, 19, 20]. The principle is to monitor the parameter (e.g., voltage droop, temperature) variations on-die before adjusting the supply voltage or clock frequency to compensate for the impact of variations. For example, [20] embeds analog voltage-droop monitors to direct the PLL to reduce clock frequency in response. However, these techniques require time to detect and react to the variations, thus only reducing a portion of the guard band for static variations [21]. Timing margin is still needed to relieve threaten from dynamic variations.

To deal with the dynamic variations, error detection and correction (EDC) techniques are proposed. Different from previous adaptive techniques that avoid timing-margin failure, EDC allows failure from dynamic variations [6, 9, 22, 23, 24, 25]. The principle is adding extra logic on the critical path to detect the timing error, then recovering from it before the circuit state is corrupted. However, existing EDC techniques have two defects in common: 1) the error detection logic often introduces considerable overhead, thus not suitable for commercial designs [6]; 2) detection and correction are required to be completed within the error cycle [26, 27], from when the error occurs (usually near half the clock cycle), therefore posing a strict constraint for large scale designs.

To overcome the above problems, we propose a novel low overhead EDC technique with relaxed error timing constraint. The contributions of this paper are listed as follows: 1) we present an error detection latch (EDL) that can detect the timing error while storing and propagating the data, with only 6 additional transistors; 2) we introduce a new detection and correction scheme that relaxes the timing constraint for error control loop by one clock cycle.

We study a case using a 16x16 multiplier targeting SMIC 55 nm process, to demonstrate the proposed technique. Post-layout SPICE simulation manifests that the proposed technique reduces the energy per cycle by 51% with 7.6% area overhead.

The rest of this paper is organized as follows. Section 2 introduces the proposed technique, in which we highlight the low overhead error detection latch (EDL) and the casual error correction (CEC) scheme. Section 3 de-

¹University of Chinese Academy of Science, No. 19(A) Yuquan Road, Shijingshan District, Beijing, 100029, China

²Institute of Microelectronics of Chinese Academy of Sciences, Beitucheng West Road, Chaoyang District, Beijing, 100049, China

a) zhuzhijiu@ime.ac.cn

b) qiaoshushan@ime.ac.cn

scribes the experiment and results. Section 4 concludes the paper.

2. Proposed technique

2.1 Error detection latch

As is shown in Fig. 1, the error detection latch (EDL) can be partitioned to two parts, a conventional latch, and an error detection unit. The error detection unit consists of two dynamic INV gates and a static INV gate. Two evaluation transistors in the dynamic INVs can share with the input tri-buffer in the conventional latch, as is marked in red and blue color, reducing the overhead for detection logic to 6 transistors.

Fig. 1. Error detection latch

The principle of the error detection unit is detecting the data transition in the high phase of the clock. In the low phase of CLK, both dynamic INVs precharge, resetting errp and errn signals. In the high phase of CLK, the dynamic INVs enter evaluation phase. If D does not transit, only one dynamic INV discharges, setting only one of errp and errn. Otherwise if D transits, both dynamic INVs discharge, setting both errp and errn, indicating the timing error.

As can be seen, the proposed EDL has the following merits:

- 1) It is compatible with conventional latch.
- 2) The overhead is only 6 transistors.
- 3) The dynamic logic is faster than static logic [28], in favor of the timing constraint for error signals

2.2 Error detection and correction scheme

We propose a simple EDC scheme to relax the timing constraint for error signals. By extending another conventional latch in the non-critical path (NCP) successive to the critical path (CP) stage, forming a basic 3-stage detection pipeline shown in Fig. 2, the error timing constraint (ETC) can be relaxed by one clock cycle. Even if the delay of the error control loop exceeds the error cycle to the next cycle, the timing error can be still corrected without corrupting the pipeline. The propagation timing of DATA and ERR signals relative to GCLK in the 3-stage pipeline is shown in Fig. 3.

As in the timing diagram of late-arrived error, due to the time-borrowing of the latch, the pipeline is not

Fig. 2. Error detection and correction pipeline

Fig. 3. Timing diagram of DATA, ERR and GCLK

corrupted although the ERR does not arrive within the error cycle. In the next cycle, the late-arrived ERR gates the clock pulse, recovering the pipeline from the timing error. The EDC scheme relaxes the timing constraint for the error control loop by one clock cycle, sufficient for large scale designs.

The OR gate for error signals in Fig. 2 is implemented as a dynamic OR tree for better timing closure, which has been proven in [29]. The structure is shown in Fig. 4.

Fig. 4. Dynamic OR tree

Once the GATE is set, the clock gating (CG) in Fig. 2 should gate the subsequent clock pulse. The circuit implementation of CG is shown in Fig. 5.

Fig. 5. Structure of clock gating

2.3 Timing constraint

The constraint in the detection and correction pipeline is different from common pipeline. According to the timing diagram in Fig. 3, the setup constraints can be summarized as:

$$T_{CP} < 1.5 * T_{clk} - T_{setup} \quad (1)$$

$$T_{CP} + T_{NCP} < 2.5 * T_{clk} - T_{setup} \quad (2)$$

It should be noted that if the path successive to the critical path is another critical path, Eq. (2) may not be satisfied. In this situation, the pipeline should extend another non-critical latch stage successive to the second critical path so that the constraint can still be satisfied.

The paths shorter than half a cycle that ends at the EDL may cause misdetection of timing errors, therefore a minimum constraint must be satisfied:

$$T_{paths_to_EDL} > \frac{1}{2} T_{clk} \quad (3)$$

3. Experiment and results

We study a case using a 16x16 pipelined multiplier to evaluate the proposed technique, targeting SMIC 55 nm CMOS technology. We first implement a baseline design at 500 MHz in 1.08 V, SS corner, and 125°C, considering the worst case variation. Thereafter another multiplier design applying the proposed technique is implemented at the same corner, in which 29 endpoint registers in the top 5% critical paths are replaced with EDLs. Both layouts of the designs are extracted with parasitic RC for accurate SPICE simulation.

Fig. 6. Simulation waveform for a delayed error signal

To demonstrate the effectiveness of dynamic variation tolerance, we run the multiplier at the typical corner with a 10% VDD droop. Fig. 6 shows the timing diagram for a multiply operation at 1 GHz. The error signal from the dynamic OR tree is delayed deliberately for one cycle to manifest the relaxed error constraint. The simulation waveform manifests that the delayed error signal gates the next clock pulse, recovering the pipeline from the timing error and producing a right output.

To evaluate the energy and performance, we operate the multiplier at the maximum frequency, fed with random operands, and measure the energy consumption per cycle. Fig. 7 shows the relation of maximum frequency and energy per cycle with supply voltage. The baseline design consumes 9.09 pJ at 500 MHz. Compared to the baseline, the EDC multiplier can run at 1100 MHz in 1.2 V, increasing the performance by 120%. Operating at the same performance with the baseline, the EDC design can scale the supply voltage to 0.95 V and consumes only 4.45 pJ

Fig. 7. Frequency and energy VS VDD

Table I. Comparison with other works

	[23] JSSC'14	[25] JSSC'15	[30] ASYN'15	[6] JSSC'18	This work
Technology	45 nm	65 nm	28 nm	40 nm	55 nm
Type	Register	Latch	Latch	Latch	Register
Area overhead	4.42	8.3%	8.4%	13.6%	7.6%
Energy reduction	45.4%	38%	40% boost frequency	45%	51%
Error timing	1 cycle	1 cycle	1 cycle	1 cycle	2 cycle

energy per cycle, reducing the energy consumption by 51%.

Table I summarizes the comparison of our work with other state of art. As can be seen, the proposed technique is superior to prior art in energy efficiency and error timing constraint.

4. Conclusion

In this paper, we propose a low overhead error detection and correction technique with relaxed error timing constraint. The EDL adds only 6 transistors to the conventional latch. The EDC scheme extends another latch non-critical stage next to the critical stage, relaxing the timing constraint for error signal by one clock cycle. A study case of a 16X16 pipelined multiplier manifests that the multiplier works correctly in the presence of delayed error propagation, showing the error timing constraint relaxed by one clock cycle. As for energy efficiency, the proposed technique reduces the energy per cycle by 51%, with 7.6% area overhead. Comparison with other works shows that the proposed technique is competitive with the state of art.

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