A 1.89 mW/Gbps SST transmitter with three-tap FFE and impedance calibration

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Abstract This study presents an 8 Gbps low-power source-series terminated (SST) transmitter for high-speed serial links. The proposed transmitter consists of a novel hybrid 20:2 multiplexer followed by a three-tap feed-forward equalizer (FFE) and a shunt path SST driver. In addition, a high-precision impedance calibration circuit with slice unit replication is proposed to match the characteristic impedance of channel, whose maximum calibration error is 0.002%. Fabricated in 55-nm CMOS technology and has area of 0.024 mm². Measurement results show that the transmitter achieves data rate of 8 Gbps while maintaining good performance. The transmitter has output swing of 510 mV with −6 dB post-tap equalization, and it consumes 15.1 mW under 1.2 V power supply.

Keywords: low-power transmitter, multiplexer, SST driver, feed-forward equalizer, impedance calibration

Classification: Integrated circuits

1. Introduction

Current-mode-logic (CML) transmitters and voltage-mode-logic (VML) transmitters are frequently used for high-speed data transmission [1, 2]. In recent years, VML transmitters have become increasingly popular. This is because whereas only a quarter of the current flows through the load in CML transmitters, the entire supply current flows through the load in VML transmitters, resulting in low power consumption [3, 4, 5, 6].

Source-series-terminated (SST) transmitters, a type of VML transmitter, have been applied in many low-power high-speed transmitters [7, 8, 9]. However, an inherent drawback of traditional SST transmitters is that their equalization capability is proportional to the power consumption [10, 11]. Therefore, when the equalization capability increases, the power consumption of the output stage also increases. As a solution, a shunting path embedded in the output driver was proposed in [12, 13], this path connects different output pins and enables current wastage during equalization to be overcome. However, two-tap feed-forward equalization (FFE) with −15.5 dB maximum de-emphasis strength limits its application for long channel loss. Thus, some sophisticated equalization circuitry with high-tap FFE has been proposed to compensate for the frequency-dependent loss of channels [14, 15]. Unfortunately, this additional complexity results in increased power consumption and area costs. So that the maximum equalization capability must be considered carefully to achieve optimum power efficiency [16, 17, 18].

Additionally, [19] proposed an analog technique instead of the conventional digital technique [20, 21] to achieve high-precision impedance matching. Three negative feedback loops were used to realize impedance calibration of pull-up, pull-down, and shunting slice units. Constant impedance of 50 Ω was achieved without setting additional slice units for worst-case process variations. However, this scheme uses four external resistors for three loops, which dramatically increases the area cost.

In this paper, a low-power SST transmitter with a three-tap FFE and slice unit replication impedance calibration scheme is presented. The transmitter can operate with data rate up to 8 Gbps, and it is fully compatible with PCI-Express 3 Gen standard. The paper is organized as follows. Section 2 describes the architectures of the proposed SST transmitter. Some related simulation results are also presented in this section. In section 3, the measurement results are discussed. Finally, a summary and the conclusion are shown in section 4.

2. Architecture and circuit implementations

Fig. 1 shows the architecture of the proposed low-power SST transmitter. It consists of a 20:2 multiplexer (MUX), a three-tap FFE, and an output driver followed by an impedance calibration circuit. The transmitter is operated at half rate and receives a half-rate clock from the on-chip PLL [22, 23]. The clock is divided and distributed for the multiplexer to provide a reference clock signal. In addition, the one-tenth clock CK/CKB with subsequent buffers serves as the clock signal for the on-chip PRBS-7 generator to provide 20-bit parallel data for the transmitter input. First the 20:2 MUX converts the parallel 20-bit data into 2-bit data named even data and odd data. Then, the even and odd data are fed into the three-tap FFE to form a series of discrete-time sequences. After that, a comprehensive combination of equalization schemes is configured to generate the pre-cursor, main-cursor, and post-cursor. Finally, these half-rate data are serialized and output with flexible swing at the output driver. Furthermore, a novel impedance calibration scheme with a slice unit replication technique is proposed to realize impedance matching that, in turn, is beneficial to power and area saving. A more detailed
implementation of the transmitter will be expatiated in the following sections.

2.1 Novel hybrid 20:2 MUX

Fig. 2 shows a detailed schematic of the novel hybrid 20:2 MUX. As is seen from Fig. 2, first a 20:10 MUX retimes and converts the 20-bit 400-Mbps data into 10-bit 800-Mbps data streams. It is achieved by a group of 10 2:1 MUXs. Each 2:1 MUX uses a 2-to-1 latch mux structure to reduce the power budget [24]. Subsequently, two parallel-connected 5:1 MUXs with five-phase clock S0–S5 serve as 10:2 MUX to generate even and odd streams. Obviously, the multi-phase clock serialization technique is also power-efficient and enables short bit periods without consuming excessive area and power for clock generation and distribution. The timing diagram among serialization clocks are also demonstrated in Fig. 2.

Fig. 2. Schematic of 20:2 MUX with the clock timing diagram

2.2 Three-tap half-rate FFE

Fig. 3(a) shows the three-tap half-rate FFE block diagram. The FFE shifter register uses three latches for the delay lines. These latches clock with CKP/CKN to shift and generate two discrete-time sequences [25, 26, 27]. Subsequently, the discrete-time sequence is converted into differential signals and fed to the FFE logic block. The FFE logic block uses an identical delay-arithmetic unit (shown in Fig. 3(b)) to configure the equalization coefficient that realizes OR, AND, XOR, and XNOR functions with the same delay so that the jitter introduced by the cell can be minimized. At the same time, half-rate pre-cursor, main-cursor, and post-cursor data are generated.

Fig. 3. Schematic of three-tap FFE (a) the three-tap FFE block diagram (b) the equalization logic circuit

2.3 Output driver

Fig. 4 shows the schematic of the output driver. It consists of 12 parallel slices, each slice includes a pre-driver and an SST driver. The pre-driver is designed to configure the equalization strength and implement the last stage serialization. Two 4:1 MUXs and a 2:1 MUX are used to finish the functions. The equalization strength depends on the combination of the mode selection code S1S0. If the mode selection code is 00, the following slice unit of the SST driver is disabled. If the mode selection code is 01, pre-cursor data are chosen for the SST slice unit. If the mode selection code is 10 and 11, main-cursor data and post-cursor data are chosen, respectively. Changing the portion of different cursors changes the equalization strength. Then, the next 2:1 MUX implements last-stage serialization and converts the single-bit data into differential signals.

The SST driver receives the data streams and outputs them with the desired swing. A shunting path connects between differential output nodes to improve the power efficiency, especially under high equalization strength. Further, the SST driver is needed to maintain 50 Ω impedance matching of the channel to obtain the optimum performance. Fig. 5 shows the detailed impedance calibration scheme.
2.4 The impedance calibration scheme
Fig. 5 shows that the impedance calibration scheme is a novel method based on an analog technique [28, 29]. Unlike conventional impedance calibration technique using a digital method [30, 31], the proposed impedance calibration scheme achieves the impedance calibration with higher precision of calibration. It includes a negative feedback calibration loop each for the pull-up slice, pull-down slice, and shunting slice impedance. The analog background calibration controls the output impedance over the PVT without an extra driver slice. Therefore, the power and area overhead can be reduced.

In the pull-up slice calibration loop, PMOS transistors M1 and M2 are in series, the calibration circuit mimics the dc operation of the pull-up slice, and the feedback loop sets the large signal dc impedance of the pull-up slice equal to one-third of $R_{cal}$ by modulating the drain-to-source impedance of M1. Due to the analog calibration schemes, only one pull-up slice is enough to achieve impedance calibration. A similar circuit is used for the pull-down slice calibration loop.

For the shunting slice calibration loop, a slice replication technique is used. In this loop, the pull-up slice and pull-down slice serve as reference resistors, and the calibration loop adjusts the dc impedance of the shunting slice by changing the drain-to-source impedance of M4. As a result, the impedance of the shunting slice is double that of the pull-up slice as well as the pull-down slice.

Fig. 6 shows the calibration output impedance results with different simulation processes, supply voltage and temperature. Fig. 6(a) and (b) respectively show the pull-up slice unit calibration results at varying supply voltage and different temperature (sweep from $-40^\circ C$ to $125^\circ C$). Correspondingly, Fig. 6(c) and (d) show the pull-down slice unit calibration results at varying supply voltage and different temperature. Also Fig. 6(e) and (f) give the shunting slice unit calibration results at varying supply voltage and different temperature. As the results demonstrate, the maximum deviations of each calibration impedance are all less than $0.01 \Omega$, where the maximum calibration errors are not more than $0.02\%$.

3. Measurement results
The transmitter is fabricated in 55-nm CMOS technology. Fig. 7(a) shows the chip micrograph. The transmitter has area of $0.024 \text{mm}^2$. The SST transmitter can operate at up to 8 Gbps under 1.2 V power supply. Fig. 7(b) depicts the simulated power breakdown for the proposed transmitter. The transmitter consumes a total power of $16.4 \text{mW}$ without equalization when working at 8 Gbps.

An on-chip PRBS-7 generator is used for producing $2^7-1$ pseudorandom bit sequence (PRBS) data pattern to the transmitter, while a Tektronix MSO71604C mixed signal oscilloscope is used to detect the differential output eye-diagram of the transmitter. Fig. 8 shows the testing PCB with 23-inch coupled micro-strip lines that act as a channel. This figure also shows its measured channel loss. It is $-4.86 \text{dB}$ at 4 GHz. Without equalization, no data eye is presented after passing through the channel due to the enormous data ISI. Fig. 9(a) shows the measured 8 Gbps eye-diagram with $-6 \text{dB}$ post-tap equalization, whose output swing is $510 \text{mV}$ and total jitter is $60 \text{ps}$. The power consumption of this mode is $15.1 \text{mW}$, whose Figure of Merit (FOM) is $1.89 \text{mW/Gbps}$. Similarly, Fig. 9(b) shows the measured 8 Gbps eye-diagram with both $3 \text{dB}$ pre-tap and $-6 \text{dB}$ post-tap equalization, whose output swing is $320 \text{mV}$ and total jitter is $65 \text{ps}$. It consumes $14.8 \text{mW}$ with the FOM of $1.85 \text{mW/Gbps}$. It is compatible with the PCI-Express 3 Gen standard. As the measurement results show,
this proposed transmitter based on shunting path, consumes lower power under high equalization strength. Table I summarizes the performance comparison with previous studies. the proposed source-series terminated transmitter has good performance on FOM.

4. Conclusion
This letter presents a low-power SST transmitter with three-tap FFE and a novel impedance calibration circuit. The three-tap FFE has $-21.5$ dB equalization capability for channel loss. A novel impedance calibration scheme based on slice replication is applied to the shunting slice calibration loop to reduce the area overhead. The transmitter is fabricated in 55-nm CMOS technology and has area of 0.024 mm$^2$. Measurement results show that the transmitter can operate at 8 Gbps while maintaining good performance.

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