The core functions of the T-attenuator is preferable compared with variable gain role in phased-array systems. For amplitude control, the 7, 8, 9, 10]. Amplitude-controllable circuit plays a key contains many transmit/receive (T/R) front-end modules. The core functions of the T/R modules include signal amplification, phase shifting, and gain controlling [5, 6, 7, 8, 9, 10]. Amplitude-controllable circuit plays a key role in phased-array systems. For amplitude control, the attenuator is preferable compared with variable gain amplifiers as it can achieve lower power consumption, lower control complexity and wider bandwidth [11, 12, 13].

In general, phased array system requires the attenuator to provide precise amplitude control (0.5 dB step in this work) and large attenuation range (15.5 dB in this work) with low insertion phase variation over the different attenuation states (<6° in this work). Generally, there are mainly three kinds of schemes to implement the attenuator. One is based on the basic type of PI-, T-topologies with embedded switches [14, 15, 16, 17, 18, 19]. [20] adopts PI/T-type topology with the SPDT/DPDT (single-pole-double-throw/double pole double throw) and series inductors to improve the cascaded matching performance, result in lower insert loss across DC-20 GHz. However, it consumes more chip size. Besides, the attenuation value is sensitive to the load variation. The third scheme is the distributed attenuator [7, 21, 22, 23, 24, 25], while it still has troubles in the attenuation ranges since it demands many transmission lines and hence consumes a large chip area [21]. Moreover, previous works have rarely discussed the amplitude/phase calibration issues of the attenuator [14, 15, 20, 21, 22, 26], since numerous components in the PI/T type attenuator and transmission lines in the distributed attenuator are particularly troublesome to realize the calibration.

The main contributions of this paper are summarized as follows.

1) The attenuator combines the PI/T-type topology with embedded switches and PI-type topology with SPDT switches to alleviate the insertion loss issue of the conventional PI/T-type topology with embedded switches in mm-wave frequency band, and achieves high attenuation range while maintaining compact chip size.

2) Amplitude/phase calibration technique is proposed in the attenuator design, thereby improving the circuit robustness and helping the attenuator achieve competitive performance compared with the state-of-the-art works.
This paper is organized as follows. Section II introduces the circuit design. In Section III, the measurement results are shown. Section IV presents the conclusions.

2. Circuit descriptions

Conventional attenuator consists of the basic 1-bit 0.5 dB, 1 dB, 2 dB, 4 dB and 8 dB attenuator stages in cascade. The process variations would have influence on the RMS amplitude error and phase variation in this case. This paper presents one amplitude calibration technique to reduce the amplitude error, which employs one different cascade strategy and extra amplitude calibration units to make the attenuation value tunable. The simulations show that the attenuator stages with 0.5 dB, 1 dB and 2 dB attenuation have small amplitude errors across 25–35 GHz in various process corners. By contrast, the attenuator stages with 4 dB and 8 dB attenuation can introduce ±0.5 dB amplitude error. Therefore, this paper splits 4 dB and 8 dB attenuation into 3.5 dB plus 0.5 dB attenuation and 7.5 dB plus 0.5 dB attenuation, respectively. The amplitude error can be manually calibrated by bypassing 0.5 dB calibration units if the measured attenuation value is higher than the desired value or cascading extra 1 dB calibration units if the measured attenuation value is lower than the desired value. This work describes the schematic of the proposed attenuator with amplitude/phase calibrations. The attenuator consists of three topologies:

1) Simplified T-type unit with embedded switch for 0.5 dB and 1 dB attenuation.
2) PI-type unit with embedded switch for 2 dB and 3.5 dB attenuation.
3) PI-type unit with the SPDT for 7.5 dB attenuation.

Two schemes are usually utilized to realize the 8 dB attenuation, including the 8 dB PI-type attenuation unit with embedded switch and two 4 dB PI-type attenuation units.
units in cascade. However, the insert loss is high due to the worse matching performance caused by the switch parasitics in CMOS. [14] introduces the series inductor to improve the matching performance, but this inductor consumes a large chip area. This paper makes a trade-off between the insert loss and chip size by adopting the PI-type unit with the SPDT in Fig. 1(b) to replace the embedded switch, for reducing the insert loss given that the matching performance is improved. As shown in Fig. 2, $C_{5}$ is inserted to compensate the insert phase variation caused by the SPDT.

Fig. 3 shows the simulated 5 basic attenuation states of the proposed attenuator and the simulated zero (reference) state of the conventional all embedded switch topology. The 7.5 dB attenuation unit uses the SPDT switch to improve the matching performance. Thus, the 0 dB reference state achieves 12.81 dB insertion loss at 30 GHz, which is improved by nearly 1.89 dB compared with the conventional all embedded switch topology. Fig. 4 and Fig. 5 show the simulated RMS amplitude error and phase variation in various process and temperature corners. The amplitude error of the 4 dB and 8 dB attenuation stages is decreased by manually reconfiguring the calibration units. The phase variation of the 2 dB and 4 dB can be decreased by manual reconfiguring the switched capacitors. The RMS amplitude error and phase variation are smaller than 0.5 dB and 2.5° over the 25–35 GHz, respectively. Especially, the proposed attenuator could achieve the RMS amplitude error of 0.13–0.25 dB if the operation frequency is limited to 26.9–31.4 GHz. The best performances of the RMS amplitude error and phase variation are 0.13 dB@29.1 GHz and 1.24°@31.9 GHz.

Table I compares the measured performance of the presented chip with the state-of-the-art works. The proposed attenuator achieves lower RMS amplitude error across 25–35 GHz due to the proposed amplitude/phase calibration. Moreover, the proposed attenuator only consumes around 0.16 mm² chip area.
When the operation frequency is limited to 26.9 GHz, this paper presents one 25 GHz attenuator and PI circuit robustness. The proposed attenuator shows the RMS amplitude error of 0.13 dB and the RMS phase variation of 1.24° across the 25–35 GHz, which is attractive for signal amplitude control in wideband micro-and millimeter-wave communication and satellite communication systems.

### Table 1. Performance comparison with previous works

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Tech. (nm)</th>
<th>Topology</th>
<th>Freq. (GHz)</th>
<th>Step (dB)</th>
<th>States</th>
<th>RMS Amp. Err. (dB)</th>
<th>RMS Pha. Var. (°)</th>
<th>Loss (dB@GHz)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]</td>
<td>180</td>
<td>Switch embedded</td>
<td>15–18</td>
<td>1</td>
<td>15</td>
<td>0.24–0.61</td>
<td>2.7–4.7</td>
<td>NA</td>
<td>0.17**</td>
</tr>
<tr>
<td>[20]</td>
<td>130</td>
<td>Using SPDT/DPDT</td>
<td>DC-20</td>
<td>1</td>
<td>32</td>
<td>&lt;0.7</td>
<td>&lt;2.5</td>
<td>~10@20</td>
<td>0.5</td>
</tr>
<tr>
<td>[21]</td>
<td>65</td>
<td>Distributed</td>
<td>50–110</td>
<td>0.75</td>
<td>14</td>
<td>NA</td>
<td>&lt;5</td>
<td>5.6@50</td>
<td>0.38</td>
</tr>
<tr>
<td>[22]a</td>
<td>180 BiCMOS</td>
<td>Distributed</td>
<td>22–29</td>
<td>1</td>
<td>16</td>
<td>0.49–0.51</td>
<td>1–4.7</td>
<td>7.9@29</td>
<td>0.94</td>
</tr>
<tr>
<td>[31]</td>
<td>130 BiCMOS</td>
<td>Switch embedded</td>
<td>DC-20</td>
<td>0.5</td>
<td>64</td>
<td>&lt;0.37</td>
<td>&lt;4</td>
<td>7.2@20</td>
<td>0.14</td>
</tr>
<tr>
<td>[32]</td>
<td>250 BiCMOS</td>
<td>Switch embedded</td>
<td>6–12.5</td>
<td>0.26</td>
<td>128</td>
<td>&lt;0.26</td>
<td>2.2–3.5</td>
<td>12.7@12.5</td>
<td>0.29</td>
</tr>
</tbody>
</table>

This work 65 Switch embedded & using SPDT 25–35 0.5 32 0.13–0.48 0.13–0.25* 1.24–2.08 12.8@30 0.16

*When the operation frequency is limited to 26.9–31.4 GHz

**Estimated according to the microphotograph. #Dual band.

4. Conclusion

This paper presents one 25–35 GHz attenuator in 65 nm CMOS. It combines the conventional PI/T topology with embedded switch and PI/T topology with the SPDT. The amplitude/phase calibration is presented to improve the circuit robustness. The proposed attenuator shows the RMS amplitude error of 0.13–0.48 dB and the RMS phase variation of 1.24°–2.08° across the 25–35 GHz, which is attractive for signal amplitude control in wideband micro- and millimeter-wave communication and satellite communication systems.

Acknowledgments

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References


