LETTER

Physical mechanism study of N-well doping effects on the single-event transient characteristic of PMOS

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Abstract N-well doping concentration plays an important role in single-event transient (SET) characteristic of transistors. While adjusting the N-well doping parameter within a proper range, it has little effect on the basic electrical performance of P-type MOSFET. The physical mechanism of well doping effects on the SET of PMOS is observed. The collapse and recovery of N-well potential, which are the critical factors that influences the SET pulse width, are analyzed by TCAD simulations. The result shows that well doping concentration could affect not only the rate of well potential recover to its equilibrium value, but the potential gradient induced by localized collapse of N-well potential between ion-strike path and source. Energy band analysis is also carried out under the triple well structure, and results show that an increase in well doping concentration will elevate the barrier of reverse-biased P-N junction and therefore cause the accumulation of holes in well, elevating the well potential, and consequently, inhibiting the parasitic bipolar amplification effect.

Keywords: single-event transient, well doping effect, parasitic bipolar amplification, energy level

Classification: Integrated circuits

1. Introduction

With the acceleration of exploring outer space, the performance of the electronic system in the space environment is becoming more and more important [1]. As more and more transistors are integrated on the same substrate, more devices will be affected when ion strikes the sensitive node. The single-event transient (SET), as well as multiple single-event transient (MSET), are induced [2, 3, 4, 5]. Since the heavy ion strike is mainly acts on the bulk region of the transistor, such as substrate and well. The characteristic of this area is an important factor which will influence the SET of transistor [6]. Thus it is necessary to study the physical mechanism of bulk area effect on the SET character of transistors in bulk silicon technology. Previous research indicates that parasitic bipolar amplification effect is the primary cause of the SET pulse-width broadening in PMOS [7, 8]. Furtherly, well potential plays an important role in this effect [9, 10], for the ion strike into transistor, the parasitic bipolar transistor is activated by well potential

collapse. In [11], it is found that the well potential expansion is not a function of the deposited charge of the heavy ion strike, but a function of the potential collapse generated by the ion strike in the well. Therefore, the key factor to improve the anti-radiation performance of transistor is how to recover the potential of well faster. Several radiation-hardening technologies have been put forward to stabilize the well potential. For example, the triple-well technology comprises a buried P-well layer that isolates the N-well from the P-type substrate [12]. This structure can inhibit the parasitic bipolar amplification effect in transistor, and consequently, reduce the SET pulse-width, meanwhile prevent the noise from substrate [13, 14]. The well potential of transistor is also affected by parasitic resistance, external voltage, doping concentration and other factors [14, 15, 16, 17]. With using the technology of radiation harden by design (RHBD) [18, 19, 20, 21], the charge collection can be effectively mitigated by introducing the guard ring contact in triple-well CMOS process [22]. Recently Zhenyu Wu found that reducing the distance between NMOS transistor and N-well can reduce N-hit SET pulse width [23]. Several works like this use layout optimization methods to maintain the stability of the N-well electrostatic potential and suppress the parasitic bipolar effect [24, 25, 26, 27, 28]. Radiation harden by process is another effective method to reduce the damage of single-event effect [9, 11]. Doping concentration of substrate, buried deep well and other area is a critical factor that could affect the charge collection induced by heavy ion incidence [13]. Although there are many analyses on the relationship between doping concentration and performance of radiation harden, few studies have been done on the physical mechanism of this relationship, and the studies related to electric potential and energy level distribution analysis are even less. After the heavy ion strike, a lot of excess non-equilibrium carriers are generated in the transistor, which results in the splitting of electron and hole quasi-fermi levels and the change of potential gradient distribution in the well region. Further research should provide physical analysis about the relationship between well doping and these changes. In addition, it was observed that in triple-well structures there exists a reverse-biased P-N junction between well and deep well of the PMOS. It is found that this junction plays an important role in charge collection of other devices [28, 29, 30]. The well electric potential has been analyzed in [11], but the factor that could affect the potential is not discussed and the rate of potential change is not analyzed. In this paper, the physical mechanism of SET

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in the transistor related to electric potential and energy level distribution in different well doping concentration was analyzed and discussed. The rate of N-well potential change was proved to be affected by well doping concentration due to its effects on the energy barrier of N-well/P+ deep well junction. The results presented in this paper provide theory guidelines for designers to optimize the SET characteristic by adjusting process parameters.

2. Model design and simulation setup

Device simulation is proved to be an effective way to study the SET pulses resulting from ion impact on transistors [31]. In this work, device model creation and ion strike simulation are performed with Synopsys Sentaurus TCAD tools. The 3-D TCAD model of PMOS was designed in a 65-nm triple-Well bulk silicon CMOS process as shown in Fig. 1. The channel length of PMOS is 65 nm, while the width of channel is 280 nm. Additionally, the size of P-type substrate is $20\ \mu\text{m} \times 20\ \mu\text{m} \times 20\ \mu\text{m}$. The N-well and the buried P+ deep well are implanted with the Gaussian doping profiles whose peak value is $1 \times 10^{17}\ \text{cm}^{-3}$, $1 \times 10^{18}\ \text{cm}^{-3}$, respectively. And the P-type substrate is doped with a constant of $1 \times 10^{16}\ \text{cm}^{-3}$. The heavy ion physical model is used to simulate the incident ion. The spatial and temporal distributions of charge around the ion track are modeled using the Gaussian radial profile [4, 5, 6]. In order to simulate the situation of different energetic particle passes through the semiconductor material, the term linear energy transfer (LET) is typically used to describe the energy loss per unit length of ion track [9]. According to the references [10, 11, 14], LET value takes $20\ \text{MeV} \cdot \text{cm}^2/\text{mg}$ as an example to simulate and compare the well doping effect on PMOS's SET pulse. In order to keep consistent with previous research, the particle incident position is selected as the center of drain, which is reported as the SET sensitive node of the off-state transistor in previous research reports [10, 11]. The physical model of all simulations is incorporated as followed: Fermi-Dirac statistics, doping dependent SRH recombination and Auger recombination, the impact of temperature, electric field, doping and carrier-carrier-scattering on mobility. In order to ensure the accuracy and reliability of the model, the I-V electrical characteristics of the PMOS model have a good agreement with SPICE model's I-V curve by adjusting the process parameters.

Fig. 1. The 3-D TCAD model and the top view of the PMOS.

3. Experiment results & analysis

In this paper, the 0.2×, 0.5×, 1×, 2×, 5× times of N-well peak doping concentration of base value $1 \times 10^{16}\ \text{cm}^{-3}$ are chosen respectively. An important principle of process optimization in radiation hardening technologies is that the fundamental electrical characteristics of transistors cannot be changed. Thus, in order to verify whether changing the N-well doping concentration will affect the electrical performance of the transistor and the accuracy of the simulation model, I-V characteristic of transistors with different concentration has been simulated and compared with SPICE model. The results in Fig. 2 indicated that the I-V characteristic of transistor model has a good agreement with the SPICE model. Besides, N-well doping concentration varies within a proper range has little influence on the electrical performance of the transistor. Therefore, it is feasible to study and optimize the radiation resistance of the transistor by adjusting the doping parameters properly. The relationship between the characteristic of PMOS's SET pulse and N-well doping concentration has been analyzed. As shown in Fig. 3, with the increase of doping concentration, the pulse width of SET is reduced consequently. This indicates that the parasitic bipolar effect is inhibited in advance by a higher doping concentration. The physical mechanism of this phenomenon, which is the focus of this thesis is to further understand how N-well doping profile affects the charge collection of PMOS.

Fig. 2. The comparison results between I-V characteristics of the transistor model at different N-well doping concentrations and the SPICE model.

Fig. 3. The SET current of PMOS with different N-well doping concentrations.

Fig. 4. (a) Cross section of PMOS device showing the horizontal cut-line through the N-well area; (b) the change of electrostatic potential along the cut-line at different times after ion strike.

3.1 Electrostatic potential analysis

After heavy-ion incidence, the electric potential in the bulk area of transistor will have a transient fluctuation. The dynamic process of N-well potential collapse after heavy ion strike is simulated. Fig. 4(b) shows that the N-well potential at different times, this plot showing that in the area of N-well below the PMOS, the collapse of potential along the cutline in Fig. 4(a) will be recovered to its equilibrium value in hundreds of picoseconds. In Fig. 4(b), the coordinate value near the zero corresponding to the area of N-well directly below the transistor. The potential of this area has the largest range of fluctuations, and then the potential outside the region gradually decrease and finally approaches the equilibrium state. This indicates that the incidence of heavy ion will lead to localized collapse of the electric potential in the N-well area. The result of this localized collapse is the activation of the parasitic bipolar amplification effect which determines the pulse width of SET. When the collapsed potential recovers to its equilibrium value, this parasitic effect will disappear. Previous studies have shown that the width of the SET pulse of the PMOS is directly determined by the time of Well potential recovery [26], but few studies have reported the factors that affect the well potential recovery speed. Next, the effect of well doping concentration on the localized collapse and recovery of well potential is further simulated and analyzed. Fig. 5 shows the comparison of N-well potential change in different doping concentrations at 100ps and 250ps after ion strike. From the analysis of this plot, N-well doping concentration with a low value will slow down the decline of N-well potential, while high doping concen-

Fig. 5. Comparison results of the recovery rate of well potential under three well doping concentrations.

Fig. 6. (a) Electron current and (b) collect electron charge of N-well contact vs. well doping concentration.

tration could accelerate. It indicates that increasing the N-well doping concentration properly can effectively reduce the well potential fluctuation and the opening time of the parasitic transistor caused by particle strike. Next, the physical background that doping influences the recovery speed of N-well potential is analyzed. According to the previous study, the N-well potential collapse after ion strike is due to the accumulation of electrons in the N-well [10]. Therefore, the recovery of N-well potential is closely related to the rate of electron removal and, thus, dramatically impacts the SET pulse-width of PMOS. Further, N-well doping effects on the rate of electron removal can also be shown in Fig. 6. In Fig. 6(a), the electron current of N-well contact is positive, indicate that the electrons are remove from N-well area. As shown in Fig. 6(b), with the increasing doping concentration, then the integral value of the current increase, indicate that more electrons are removed. In addition, the peak value of electron current is large at the beginning of ion strike, indicates that higher doping concentration of the well will helps the electron remove faster from N-well, and then stabilizes the well potential quickly. When ion strikes the PMOS transistor, the original potential equilibrium state in N-well will be broken, and an extra large number of non-equilibrium carriers will be produced. Then, under the influences of funnel effect and electric field, the additional non-equilibrium carrier will drift and diffuse in N-well and other region. Finally, the deposited charge will be collected by ports of PMOS device and this charge collection will generate transient current, as Fig. 7 shown. In Fig. 7, after the peak of SET current, the absolute value of source current is relatively higher than the absolute value of drain. It was attributed to the parasitic bipolar amplification effect. Furthermore, the degree of local potential collapse, in other words, the potential and carrier concentration gradient in the ion-strike region determines the source current. Ion strike the PMOS will cause the N-well electron potential to drop significantly below supply voltage, termed well collapse, resulting in this effect. When the parasitic transistor opens, the source injected a large number of holes into N-well, which is why the SET pulse of PMOS have a “long-tail” area. Transient current of source will also change with the variation of N-well concentration. Physical mechanism of this change was analyzed below by making a slant cut-line of well potential from source to N-well in TCAD, as shown in Fig. 8(a). After ion strike, the N-well voltage drop will create a potential gradient

Fig. 7. SET currents of all the ports of PMOS

Fig. 8. (a) Oblique cut-line of electrostatic potential from source to ion strike path; (b) the distribution of electrostatic potential along the cut-line in (a).

between the strike path and the source contact. The result of this potential gradient is the hole current flow in the N-well. As it is shown that in Fig. 8(b), the gradient of potential is relative to N-well doping concentration. Higher concentration within a proper range will reduce this potential gradient. As shown in Fig. 9 that with the increase of the concentration, the hole current of source will reduce accordingly.

Fig. 9. The distribution of hole current density from source to ion strike path along the cut-line in Fig. 8(a).

3.2 Band structure analysis

Another important factor which will affect the N-well potential is the reverse-biased P-N junctions at the interface of N-well/P+ deep well. Triple well technology in CMOS manufacturing process comprises a buried P+ well layer that isolates the N-well from the p-substrate. Because of this isolation, noise signal and CMOS latch-up susceptibility will be reduced. Meanwhile, the N-well potential will

Fig. 10. (a) Vertical cut-line in cross section of PMOS transistor; (b) Energy band structure of reverse-biased P-N junction between N-well and P+ deep well without ion striking;

Fig. 11. Energy band structure of P-N junction at the time of 50 ps after ion striking.

also be isolated. Therefore, it is necessary to study the P-N junction effects on the N-well potential fluctuations. Fig. 10 and Fig. 11 show the energy band of the reverse-biased P-N junction along the vertical direction of the PMOS before and after the ion strike by extracted from energy band analysis tools in TCAD. As shown in Fig. 10(b), N-well energy band is on the left while P+ deep well energy band is on the right. Affected by the reverse voltage, the location of hole's quasi-fermi level is higher than electron's, this is consistent with the conclusion of conventional semiconductors. In Fig. 10(b), outside of depletion layer region, the quasi-fermi levels of both hole and electron are essentially coincident. After heavy ion strike, the quasi-Fermi level of hole E_F^p and electron E_F^n are separated from each other, while E_F^n is near the bottom of conduction band, and E_F^p is near the top of valance band, as shown in Fig. 11. According to the knowledge of semiconductor physics, the concentration of electron and hole in non-equilibrium state can be determined by the following classical formulas.

$$n = n_i \exp\left(\frac{E_F^n - E_i}{k_0 T}\right) \quad (1)$$

$$p = n_i \exp\left(\frac{E_i - E_F^p}{k_0 T}\right) \quad (2)$$

where p and n are the non-equilibrium concentration values of hole and electron, respectively. n_i is the concentration of

carriers in pure silicon, and E_i is Fermi-level of the intrinsic semiconductor. k_0 is Boltzmann constant, T is temperature. By combining the above two equations, the following equation can be obtained, as shown in equation 3.

$$np = n_i^2 \exp\left(\frac{E_F^n - E_F^p}{k_0 T}\right) \quad (3)$$

It will derive from equation (3) that the separation of E_F^n and E_F^p can lead to an increase in the non-equilibrium carrier concentration. From above analysis, two diverge quasi-fermi level indicate that in N-well, at the beginning of ion strike, the concentration of hole and electron can reach high values at the same time, and then converge gradually until it reaches the equilibrium state, as shown in Fig. 9. The simulations and analysis proved that ion strike will generate many coexist non-equilibrium carriers in N-well. The lifetime of these carriers and recovery time of the well potential decide the SET pulse width in the MOSFET. Besides, it is shown that reverse-biased P-N junction in Fig. 11 generate a potential barrier between N-well and substrate. This potential barrier could obstruct the carriers drift into the opposite side, and will localize the fluctuation of N-well potential in N-well area to a certain extent. After ion strike the transistor, a large number of non-equilibrium carriers will be produced and coexist in both N-well and P+ deep well. Next the N-well doping concentration influence on the drift of carriers is simulated, as shown in Fig. 12. When the doping concentration of N-well increases, the height of the potential barrier will elevate, furtherly inhibiting the carrier drift through the potential barrier. In this case, the number of holes drifting into substrate will be reduced, which will lead to the accumulation of holes in N-well, thus improving the well potential and inhibiting the parasitic bipolar amplification effect. As shown in Fig. 13, the hole collect charge of substrate contact almost coincides with the total charge collected, since the N-well/P+ well junction is reverse biased, only the minority carriers in the N-well are collected in the P+ region. This indicated that in the process of SET in PMOS, only the holes can enter the substrate and be collected.

Fig. 12. Energy band structure of reverse-biased P-N junction in N-well/P+ deep well interface under different N-well doping concentrations at the time of 50 ps after ion striking.

Fig. 13. The collect charge of the substrate in PMOS at different N-well doping concentrations.

4. Conclusion

In this paper, the relationship between SET pulse width and N-well doping concentration was studied by physical analysis. With the well-doping concentration increasing, the potential gradient between source and ion striking path is reduced to weaken the hole collection of source contact, and then reduce the pulse width of SET. For the triple well technology, results show that an increase in well-doping concentration will elevate the barrier of reverse-junction and therefore reduce the passing carriers. The N-well potential will be elevated by the accumulate of holes in well. These analysis results give designers insight into the physical mechanism of transistor's SET behavior in process variations.

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