A 3rd-order 1-bit $\Sigma$-$\Delta$ modulator with a 2-tap FIR filter embedded

Xiao Chen$^1$, Zhi-gong Wang$^{1a}$, and Fei Li$^{1b}$

Abstract This paper presents a low-voltage 3rd-order single-bit switched-capacitor $\Sigma$-$\Delta$ modulator implemented in a 40-nm CMOS technology. In the modulator, a 2-tap FIR (finite impulse response) filter is employed in the feedback loop to reduce the integrator output swings. With the help of digital assisted techniques, the number of the sampling capacitors in the first integrator is reduced to mitigate the performance deterioration caused by capacitor mismatch. Besides, the inverter-based amplifiers with dynamic-biased structure are proposed to reduce the power consumption. The proposed modulator is sampled at 25.6 MHz over a bandwidth of 100 kHz. The modulator achieves a max SNR (signal-to-noise ratio) of 92.1 dB, a max SNDR (signal-to-noise and distortion ratio) of 87.3 dB, and a DR (dynamic range) of 88.1 dB under the supply voltage of $\pm 0.45$ V while consuming a total power consumption of 790 $\mu$W.

Keywords: low-voltage, $\Sigma$-$\Delta$ modulator, 2-tap FIR filter, inverter-based amplifier

Classification: Integrated circuits

1. Introduction

The $\Sigma$-$\Delta$ modulators could provide a relatively high SNR (signal-to-noise ratio) in the low frequency bands by using oversampling and noise-shaping techniques [1, 2, 3, 4, 5, 6], and they have been broadly employed in many portable electronic products. With the development of nanometer CMOS technology, the supply voltage of integrated circuits is becoming lower and lower. When moving into sub-1 V environment, the characteristics of a MOSFET such as intrinsic gain and cut-off frequency degrade sharply, which shows that the design of a low voltage analog circuit is a challenging task [7, 8, 9]. Thus, it is very meaningful to research the implementation of a $\Sigma$-$\Delta$ modulator under sub-1 V environment.

A low-voltage low-power 3rd-order single-bit switched-capacitor $\Sigma$-$\Delta$ modulator with a 2-tap FIR filter embedded is presented in this paper. With the help of digital techniques, there are fewer sampling capacitors utilized in the first integrator compared to the traditional one. Thus, the performance deterioration caused by capacitor mismatch could be mitigated. In addition, the dynamic-biased inverter-based amplifiers are employed to reduce the total power consumption. Therefore, the modulator performance is improved.

The rest of this paper is organized as follows. Section 2 describes the architecture and schematic realization of the modulator. Section 3 explains the key building blocks in detail. Section 4 discusses the simulation results and Section 5 draws the conclusion finally.

2. System level design and circuit implementation of the modulator

2.1 The modulator architecture

When designing a low voltage $\Sigma$-$\Delta$ modulator, the feed-forward topology is usually a good choice [10, 11, 12] for both power consumption and performance reasons: firstly, the output swings of the integrators are much smaller than those of feedback architecture, which means the total power consumption could be reduced. Secondly, the gain requirement for the operational amplifier is more relaxed than that of feedback architecture, which implies that there is no need to design a high-gain amplifier in low voltage environment [13, 14, 15]. In order to reduce the power consumption further, the output swings of the first integrator should be as small as possible. The reason is that the first integrator often consumes more than half of the total power consumption [16, 17]. For single-bit modulator, inserting an FIR filter into the feedback loop is an effective way to reduce the output swings because the integration step could be attenuated [18, 19, 20]. In this design, the 2-tap FIR filter is selected because some coefficients are too small to implement in the modulator embedding the multi-tap FIR filters [20].

Fig. 1(a) shows the proposed $\Sigma$-$\Delta$ modulator structure. Compared with the traditional feed-forward single-bit modulator depicted in Fig. 1(b), a 2-tap filter is inserted in the feedback loop. It should be pointed out that the filter introduces an additional pole in the NTF (noise transfer function) of the modulator, which degrades the effect of noise shaping. Thus, a compensation loop is designed accordingly [20]. The histogram of the integrator output swings in the first stage are displayed in Fig. 2. It can be referred that the output swings are suppressed in the modulator with the filter embedded.

2.2 Circuit realization of the $\Sigma$-$\Delta$ modulator

The complete modulator schematic is shown in Fig. 3. The power rail VDD and VSS are defined as 0.45 V and $\pm 0.45$ V respectively, and the common mode voltage is set to 0 V (GND). The bandwidth of input signal is 100 kHz, and the OSR (oversampling ratio) is chosen as 128. After careful calculation and optimization, $C_1$ is set to 2.8 pF to overcome the influences caused by $kT/C$ noise.
The values of all the capacitors are shown in Table I. It can be found that $C_{s2b}$ and $C_b$ are too small to be implemented directly. Thus, they are made up by several larger capacitors in series. In addition, bootstrapped switches [24, 25] are utilized at the input of the modulator to improve the linearity of sampled signals. The clock timing waveform is given in Fig. 4.

![Fig. 1](image1.png)  
(a) The structure with a 2-tap FIR embedded.

![Fig. 2](image2.png)  
(b) The conventional structure.

**Fig. 1.** The feed-forward single-bit ΣΔ modulator.

![Fig. 2](image3.png)  
Fig. 2. The histogram of the first integrator output swings in the modulators.

![Fig. 3](image4.png)  
Fig. 3. Complete schematic of the proposed ΣΔ modulator. ▼: Bootstrapped switch, □: Normal CMOS switch

<table>
<thead>
<tr>
<th>Table I. Capacitor values (Units: pF).</th>
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<tbody>
<tr>
<td>Sampling Capacitors</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>$C_{d1}$ = 2.8</td>
</tr>
<tr>
<td>$C_{d2}$ = 0.1</td>
</tr>
<tr>
<td>$C_{d3} = 0.0125$</td>
</tr>
<tr>
<td>$C_{d4} = 0.1$</td>
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</table>

![Fig. 4](image5.png)  
Fig. 4. The clock timing waveform.
3. Significant building blocks in the modulator

3.1 The integrator with 2-tap FIR filter embedded

Fig. 5 shows a conventional integrator with the 2-tap FIR filter embedded [20]. The integrator is realized in an analog way and there are 4 sampling capacitors utilized in total. However, the value of these capacitors is very large, which means a large area occupied. Also, the mismatch of these capacitors will deteriorate the modulator performance. In order to solve these problems, the integrator with only 2 sampling capacitors is proposed in this paper, as shown in Fig. 3. The single-ended type is given in Fig. 6 for the convenience in analyzing its working principle.

When at the end of nth sampling phase, the charges on $C_{s1}$ and $C_{s2}$ are $C_{s1} V_{in} (n - 1/2)$ and $C_{s1} V_{in} (n - 1)$ respectively. At the end of nth integration phase, the charges on the $C_{s1}$ and $C_{s2}$ are $C_{s1} V_{fb} (n)$ and $C_{s1} V_{o1} (n)$. According to the principle of charge conservation,

$$C_{s1} V_{in} (n - 1/2) + C_{s1} V_{in} (n - 1) = C_{s1} V_{fb} (n) + C_{s1} V_{o1} (n)$$

(1)

Take the z-transfer transform on Eq. (1) and solve $V_{o1} (z)$, we can obtain

$$V_{o1} (z) = V_{o1} (z) z^{-1} + \frac{C_{s1}}{C_{s2}} V_{in} (z) z^{-1/2} - \frac{C_{s1}}{C_{s2}} V_{fb} (z)$$

(2)

The z-transfer form of Eq. (3) is

$$P_{n[1:0]} = P(z) + P(z) z^{-1} - P(z) (1 + z^{-1})$$

(4)

Since there are 2 addends in Eq. (4), the feedback reference voltage should be divided by 2, and $V_{fb}(z)$ is expressed as

$$V_{fb} (z) = P(z) (1 + z^{-1}) \frac{VDD}{2}$$

(5)

The final expression of $V_{o1} (z)$ is

$$V_{o1} (z) = V_{o1} (z) z^{-1} + \frac{C_{s1}}{C_{s2}} V_{in} (z) z^{-1/2} - \frac{C_{s1}}{C_{s2}} \frac{(1 + z^{-1})}{2} P(z) VDD$$

(6)

Eq. (6) shows clearly that the 2-tap FIR filter is embedded in the feedback path of the integrator.

Compared with the integrator presented in [20], there are fewer sampling capacitors employed in the proposed integrator. Hence, the area of the integrator is reduced and the performance deterioration caused by capacitor mismatch could be alleviated.

3.2 The dynamic-biased inverter-based amplifiers

In sub-1 V environment, the inverter-based structure is very popular for the amplifier design because it has a higher $g_m/i_d$ efficiency and a larger input common voltage range [19, 26]. In this paper, a two-stage inverter-based amplifier with Miller compensation is utilized, as shown in Fig. 8. In the first stage, both PMOS (M1 and M2) and NMOS (M3 and M4) are used as input differential pairs, and M0 plays the role as the current source. Different from the inverter-based amplifier displayed in Fig. 9 [26], the bottom transistor controlled by $V_{emh}$ is split into two and placed parallel with the NMOS input pairs. Besides, the sources and bodies of the PMOS input pair are connected together to avoid the body effect. Thus, the output voltage swings of the first stage is improved, and M0 is easier to keep in saturation region. The second stage of the amplifier are just simple inverters made up by M6~M8. $R_s$ and $C_v$ are employed to improve the phase margin. The DC gain of the proposed amplifier could be derived as

$$A_v = \frac{(g_{m1.2} + g_{m3.4})(g_{m6.8} + g_{m7.9})}{(g_{d1.2} + g_{d3.4} + g_{d3.4} + g_{d6.8} + g_{d7.9})}$$

(7)

where $g_m$ and $g_{ds}$ are the trans-conductance and output admittance of the transistor respectively. The frequency responses over PVT (process-voltage-temperature) variations of the amplifier are given in Fig. 10. The temperature range is from 0°C to 85°C and the voltage variation is ±10%. The DC gain and GBW at 27°C under the typical corner is 53.8 dB and 148 MHz respectively, and the corresponding phase margin is 58°.
During the whole working process of the $\Sigma$-$\Delta$ modulator, the amplifier should be settled within the required range during the integration phase and it just needs to hold the voltage during the sampling phase. Thus, the amplifier could be closed during the sampling phase to reduce the total power consumption. However, if the amplifier is closed completely [27], the output voltage of the integrator could not be held precisely because of the leakage current. Consequently, the modulator performance will deteriorate. Therefore, the amplifier is just closed partly during the sampling phase. In Fig. 11, the proposed amplifier is split into two switch-controlled parts. The first amplifier is working during both sampling phase and integration phase, while the second amplifier is only working during the integration phase. Hence, about 50% power consumption of the amplifier could be reduced during the sampling phase. Moreover, the amplifiers used in other stages also adopts the same structure. Therefore, the total power consumption is further reduced.

### 4. Post-layout simulation results

The proposed $\Sigma$-$\Delta$ modulator is designed in a 40-nm CMOS process. The layout of the modulator is shown in Fig. 12, and the core area is 0.135 $\mu$m². The post-layout output PSD (power spectrum density) is depicted in Fig. 13. The max SNR and max SNDR (signal-to-noise and distortion ratio) are 92.1 dB and 87.3 dB respectively, with a 95 kHz sinusoid input signal. The relationships between SNR/SNDR and normalized input are given in Fig. 14. The DR (dynamic range) is 88.1 dB. The modulator consumes a total power of 790 $\mu$W. The performance summary of the proposed modulator is compared with previous several-hundred-kHz BW works with the near 1 V supply in Table II. The proposed modulator achieves the best FOM (figure-of-merit) among these works.

**Fig. 8.** The two-stage inverter-based amplifier presented in this paper.

**Fig. 9.** The inverter-based amplifier presented in [26].

**Fig. 10.** Frequency responses of the proposed amplifier over PVT variations.

**Fig. 11.** The operational amplifier with switch-controlled parts.

**Fig. 12.** Layout of the $\Sigma$-$\Delta$ modulator.
over a bandwidth of 100 kHz. The total power consumed is 790 µW under the supply voltage of ±0.45 V.

Acknowledgments
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References
[20] Z. Yang, et al.: “A 0.7-V 100-µW audio delta-sigma modulator

Table II. Performance summary of the several-hundred-kHz BW ΣΔ modulators with near 1 supply.

<table>
<thead>
<tr>
<th>References</th>
<th>[28]</th>
<th>[29]</th>
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<tr>
<td>Process (nm)</td>
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<td>1.2</td>
<td>0.6</td>
<td>1.2</td>
<td>0.9 ±0.45</td>
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<td>100</td>
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<tr>
<td>Power (mW)</td>
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<td>DR (dB)</td>
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<td>87.7</td>
<td>76</td>
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<td>FOM (dB)</td>
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<td>163.9</td>
<td>166.6</td>
<td>164.2</td>
<td>169.1</td>
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</table>

FOM = DR + 10lg(BW/Power)

5. Conclusion
A 3rd-order 1-bit Σ-Δ modulator with a 2-tap FIR filter embedded is presented in this paper. The modulator is designed and implemented in a 40-nm CMOS technology. In order to reduce output swings of the first integrator, a 2-tap FIR filter is embedded. The FIR filter is realized in a digital way and thus the number of sampling capacitors in the first stage is reduced. Moreover, the inverter-based amplifiers employing the dynamic-biased structure are proposed to reduce the total power consumption. The max SNDR and DR are 87.3 dB and 88.1 dB respectively...


