Power and thermal management in SRAM and DRAM using adaptive body biasing technique

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Abstract Low power and thermal design techniques are more advantageous for high-performance memory cells. Body bias is an adaptive technique used for power and thermal management in memory systems. It offers an efficient solution for the memory’s power and thermal problems. In this study, a thermal management controller is presented as a complete hardware tuning loop. The controller is applied on both Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) units that actively monitors and controls the temperature via the power dissipation control in both memory types. The proposed combined circuits within the tuning loop are able to reduce the high power and temperatures, and dragging it around safe limits to avoid chip hardware damages. Results confirm that, the power dissipation of 6T SRAM cell is reduced by 9.77%, while the power of 1T1C DRAM cell is reduced by 8.50%. Thermal reduction was in the range of (5°C–10°C) per each body bias step voltage.

Keywords: thermal management, body biasing, power reduction, voltage scaling

Classification: Integrated circuits

1. Introduction

The dramatically performance increase of memory systems lead to a significant increase of power consumption in active and idle memory units, resulting in higher operating temperatures within memory cells. Subsequently, the highly dissipated power and temperatures may prohibit or restrict the ability and reliability of overall system’s performance. Therefore, for design memory systems, power and thermal management issues have become prominent aspects for computer system manufactures which is necessary to maintain safe power and temperature levels [1, 2].

Low power/thermal design techniques are more advantageous for high-performance memory systems. Body bias is a low power/thermal management technique used in memory systems. It offers an efficient solution for the memory’s power/thermal problems based on CMOS building blocks and circuits. Adaptive body bias technique is efficient for controlling the power dissipation and temperatures of memory systems for both SRAM and DRAM units [3].

In this study, a thermal management controller is presented as a complete hardware tuning loop. The controller is applied on both Static Random Access Memory (SRAM) and Dynamic Random access memory (DRAM) units that actively monitors and controls the temperature via the power dissipation control in both memory types.

The presented tuning loop is able to reduce the high power and temperatures and dragging it around safe limits to avoid chip hardware damages. All the controller inner blocks operate on the leakage current reduction for the continuous scaling of temperatures in CMOS devices. It has been confirmed that a potential saving of power dissipation reduction has been obtained by (9.77%) and (8.50%) for SRAM and DRAM respectively when compared with no body bias readings. The thermal reduction was in the range of (5°C–10°C) per each body bias step voltage.

Because of the ever faster clock speeds and simultaneously smaller physical enclosures; power and thermal management for memory cells have emerged as a key challenge and constrain problems during the last several decades. The challenges posed to make power and thermal management of SRAM and DRAM memories as a vital technology in the continued development of computer and digital systems and it has strong face validity in recent publications [4].

H. Shin, and E. Chung in [5] proposed two management algorithms for in-DRAM caches in order to achieve low-latency and low-power 3D-stacked DRAM device. Through the computing system simulation, the improvements of energy delay product were higher than 67%. K. Gavaskar in [6] applied different techniques to SRAM cell to reduce leakage power without affecting its performance. A novel SRAM (10T) architecture is proposed which operates in three modes (active, park, standby or hold). The main objective of the proposed architecture is to provide better stability and reduced delay in active mode, reduced leakage current in standby mode and retaining the logic state in park mode, different design metrics are taken into consideration.

Li-Jun Zhang et al. in [7] applied body biasing, source biasing, dynamic VDD, negative wordline, and bitline floating schemes by controlling different terminal voltages of the SRAM cell in standby mode. To validate the effectiveness of low power techniques, the leakage current, static noise margin, and read current of SRAM cells, based on the UMC 55nm CMOS process with leakage current reduction techniques has been simulated. Results indicate

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that, using dynamic $V_{DD}$ and source biasing schemes, greater leakage suppressing capability, can be obtained. P. Gupta et al. in [8] presents a novel 8T SRAM cell with access pass gates replaced with modified PMOS pass transistor logic. Their work proposes functional SRAM cell at 45 nm technology with improved stability for sub-threshold operation and is attractive for low power based application in the scaled technology. Finally, D. Sulaiman et al. in [9] proposed an adaptive supply and body voltage control by applying optimum $V_{dd}$ and body voltages to the microprocessor unit, which compensate the threshold voltage and clock frequency for ultra-low power design, in order to achieve optimal power/temperature solution; they proposed a tuning loop that has been designed and tested with different simulation environments, and for different temperatures. In [10] Particle Swarm Optimization (PSO) algorithm and Pareto Front (PF) solution are used to evaluate and confirm the simulated $V_{th}$-$V_{dd}$ combination sets for optimal power reduction.

2. Sources of power dissipation in CMOS circuits

The two main sources of power dissipation in CMOS circuits are; dynamic and static power dissipation. Dynamic power due to charging and discharging load capacitances, and static power dissipation due to leakage currents when transistors in the idle/off states [11]. The power dissipation in a CMOS inverter is shown in Fig. 1. The average dynamic power can be expressed as [12, 13]:

$$P_{\text{dynamic}} = \frac{1}{T} \int_0^T i_{dd}(t) V_{dd} \, dt = \frac{V_{dd}}{T} \int_0^T i_{dd}(t) \, dt$$  \hspace{1cm} (1)

where $i_{dd}(t)$ is the transient current drawn from the power supply and $V_{dd}$ is the supply voltage. The integral is the total charges delivered during the time interval $T$.

Assuming a nodal activity of $\alpha$ on the load ($C_L$) and a clock frequency of $f$, the total number of transitions amounts to $(\alpha f T)$. Therefore, Eq. (1) is simplified [14]:

$$P_{\text{dynamic}} = \frac{V_{dd}}{T} \alpha f C_L = \alpha C_L V_{dd}^2 f$$  \hspace{1cm} (2)

The static power is associated with maintaining the logic values of internal circuit nodes between the switching events. It depends mainly on current leaks through transistors when they are turned off [15]. The leakage power can be formulated as:

$$P_{\text{leakage}} = I_{\text{leakage}} V_{dd}$$  \hspace{1cm} (3)
\[ I_{\text{sub}} = \mu C_{\text{ox}} \frac{W}{L} V_{T}^{2} \left( e^{\frac{V_{GS} - V_{T}}{C_{0}}} \right) \left(1 - e^{\frac{-V_{DS}}{C_{0}}} \right) \]  
(6)

\[ V_{T} = \frac{KT}{q} \]  
(7)

Where \( \mu \) is the carrier mobility, \( C_{\text{ox}} \) is the oxide capacitance per unit area, \( W \) is the transistor width, \( L \) is the transistor length, \( V_{GS} \) and \( V_{DS} \) are the gate to source and drain to source voltage respectively, \( V_{th} \) is the threshold voltage, \( K \) is the Boltzmann constant, \( q \) is the unit charge, \( T \) is the absolute temperature and \( V_{T} \) is the thermal voltage [23].

Increasing of threshold voltage \( V_{th} \) tends to exponentially decrease the sub-threshold leakage currents. The reverse body biasing (RBB) technique is the only technique in the circuit level to increases the threshold voltage, consequently reduces leakage power dissipation [24].

4. Design and implementation

Body biasing is considered as a power and temperature aware technique. Sub-threshold leakage is expected to contribute overall power consumption in high performance designs. In the circuit level, reducing the sub-threshold leakage currents which is temperature dependent caused by reduction in \( V_{th} \) while attaining the circuit high performance. RBB is used to dynamically increase the threshold voltage of MOSFETs, thereby reducing the leakage power and temperature [25]. Based on sub-threshold leakage current variations, the thermal aware controller for 6T SRAM and 1T1C DRAM cells are proposed. The circuit diagram of \( I_{\text{sub}} \) monitoring circuit for SRAM and DRAM is shown in Fig. 4.

In order to sense the sub-threshold leakage current in 6T SRAM cell without affecting the state stored in the cell, a specific inverter is added and connected in parallel with one side of 6T SRAM cell with the same transistor specifications used within the cell. \( I_{\text{sub}} \) is highly increasing with temperature and when the temperature of SRAM cell reaches the maximum range, the controller is start to operate. \( I_{\text{sub}} \) in a DRAM cell is directly sensed by the leakage between the source of NMOS transistor and the capacitor, it has very accurate values.

The current mirror is used to amplify the monitored \( I_{\text{sub}} \) in both SRAM and DRAM cells and instead of a low current value, an op-amp with feedback resistor is used as a current to voltage converter that converts \( I_{\text{sub}} \) into output voltage \( (V_{o}) \) [26].

\[ V_{o} = -I_{\text{sub}} R_{f} \]  
(8)

Fig. 5. Shows the proposed block diagram of Power/thermal aware controller for 6T SRAM cell and 1T1C DRAM cell.

The antilog/exponential amplifier is used to amplify the voltage exponentially from the temperature monitoring circuit [27]. In order to operate the controller circuit in the fast and accurate response, the voltage from antilog is converted to a clock frequency using current-starved voltage-controlled oscillator (CS-VCO) circuit to maintain a constant amplitude level and oscillation [28]. The oscillation frequency of the current starved VCO can be determined by the following equation [29]:

\[ V_{o} = \frac{1}{N(t_{1} + t_{2})} = \frac{1}{NC_{\text{tot}}V_{dd}} \]  
(9)

The nominal voltage is converted to a frequency and compared to the frequency from leakage monitoring circuit which is the temperature dependent using a phase detector (PD) circuit to produce required body bias voltages [30].

The high frequencies and fast temperature variations of SRAM and DRAM cells lead to generate a ripple voltage in the phase detector outputs. Therefore, the controller requires a Low Pass Filter (LPF) to convert this rippled voltage to a stable voltage quickly. The LPF circuit converts the voltage from phase detector circuit to desired body bias voltages for type of memory cells in order to minimizing the dissipated power and temperatures. Therefore an accurate RC passive filter has been designed.
All the design calculations and measurements are achieved according to the desired values for each block based on the 45-nm technology, low power predictive model to evaluate the theoretical basics and fundamentals, it confirms satisfactory results.

5. Results and discussion

All internal blocks of the combined block diagram of the tuning loop shown in Fig. 5 are designed using 45 nm Low Power Predictive Model (45 nm-LPTM) for different temperatures and simulated to generate adaptive body bias voltages for power and thermal management in SRAM and DRAM cells. The complete model for the proposed controllers are shown in Fig. 6 and Fig. 7.

The output voltages drawn from 6T SRAM and 1T1C DRAM monitoring circuits are measures for the temperature range (30–80) °C. \( V_{\text{out}} \) versus temperatures for \( I_{\text{sub}} \) monitoring circuits is recorded in Table I.

The reset circuit for both reference frequencies \( f_{\text{ref}} \) and temperature dependent frequency \( f_{\text{in}} \) is shown in Fig. 8 to reset both frequencies in 1 µs intervals, and the phase detector model is shown in Fig. 9.

The LPF and voltage follower are used to obtain the average voltage variation to eliminate any ripple factors added to the body bias voltage. The input/output voltage characteristics of antilog amplifier versus temperature ranges is presented in Table II.

To demonstrate the operation of PD for the phase difference between \( f_{\text{ref}} \) and \( f_{\text{in}} \), three cases are studied: \( \Delta \phi = 0, \Delta \phi = \pi/2 \), and \( \Delta \phi = 0 - \pi/2 \).

Results when \( \Delta \phi = 0 - \pi/2 \) is shown in Fig. 10.

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**Table I.** The selected values of \( V_{\text{ref}} \) and obtained \( f_{\text{ref}} \)

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>( V_{\text{out}} ) (MV)</th>
<th>( f_{\text{ref}} ) (MHz)</th>
<th>( V_{\text{ref}} ) (mV)</th>
<th>( f_{\text{ref}} ) (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRAM</td>
<td>435</td>
<td>293</td>
<td>410</td>
<td>550</td>
</tr>
<tr>
<td></td>
<td>792</td>
<td>319</td>
<td>722</td>
<td>950</td>
</tr>
<tr>
<td></td>
<td>408</td>
<td>275</td>
<td>410</td>
<td>550</td>
</tr>
<tr>
<td>DRAM</td>
<td>623</td>
<td>286</td>
<td>506</td>
<td>750</td>
</tr>
<tr>
<td></td>
<td>710</td>
<td>305</td>
<td>722</td>
<td>950</td>
</tr>
</tbody>
</table>

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**Fig. 6.** The 6T SRAM power & temperature tuning loop

**Fig. 7.** The 1T1C DRAM power & temperature tuning loop

**Fig. 8.** The Reset circuit model

**Fig. 9.** The phase detector (PD) model

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by (9.77%) and (8.50%) for SRAM and DRAM respectively, and the potential saving of percentages of the power dissipation reduction has been obtained by (9.77%); starting from (5.89%) up to (13.13%) per each body bias step voltage. While, the potential saving of percentages of the power dissipation reduction in DRAM has been obtained by (8.50%); starting from (4.71%) up to (12.23%) per each body bias step voltage. The thermal reduction was in the range of (5°C–10°C) per each body bias step voltage.

6. Conclusion

The proposed loop has been designed completely and tested with different simulation environments, and for different temperatures. Results confirmed significant improvements of both power and temperatures. Power dissipation reduction in SRAM has been obtained by (9.77%); starting from (5.89%) up to (13.13%) per each body bias step voltage. While, the potential saving of percentages of the power dissipation reduction in DRAM has been obtained by (8.50%); starting from (4.71%) up to (12.23%) per each body bias step voltage. The thermal reduction was in the range of (5°C–10°C) per each body bias step voltage. These results show the greatest promise in effectively power and thermal management in SRAM and DRAM cells.

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References


