A 0.8–3.4 GHz process variation insensitive duty-cycle corrector for high-speed memory I/O links

Heejae Hwang and Jongsun Kim

Abstract This Letter presents a 0.8–3.4 GHz process variation insensitive full-swing duty-cycle corrector (DCC) for high-speed memory I/O links. The proposed DCC utilizes a new full-swing duty cycle adjuster (DCA) that can provide a full-swing output clock of 50% duty-cycle without using a small-swing to full-swing level shifter. The proposed full-swing DCC is based on a new pseudo-differential feedback delay element (PFDE) and fundamentally eliminates the problem of increased duty-cycle errors due to the use of a level shifter that is vulnerable to process corner variation. The proposed DCC is implemented in a 40-nm CMOS process and achieves an operating frequency range of 0.8–3.4 GHz. The duty-cycle correction range is ±15% at 3.4 GHz. The DCC dissipates 2.8 mW from a 1.0 V supply at 3.4 GHz and occupies an active area of only 0.0054 mm².

Keywords: duty-cycle corrector, memory interface, LPDDR5, DRAM

Classification: Integrated circuits

1. Introduction

As the memory bandwidth required for mobile devices and computing systems for big data processing such as cloud computing and artificial intelligence (AI) increases, the operating frequency of the memory I/O link is continuously increasing. Recent high-speed DRAMS [1, 2, 5, 6, 7, 8, 9, 10] and memory controllers [3, 4] operating above multi-Gbps demand very precise 50% on-chip duty-cycle clocks to improve timing margins. However, the clock duty-cycle of a memory system is distorted by impedance mismatches, dispersion and crosstalk noise that occur in memory interface channels operating above multiple GHz. In addition, when a high-speed small-swing differential clock signal passing through the off-chip memory interface reaches the DRAM, this small-swing signal is usually converted to full-swing clock through an on-chip input clock buffer. However, this input clock buffer can cause additional duty-cycle errors due to variations in process, voltage, and temperature (PVT).

To eliminate the clock duty-cycle errors in memory interface channels, input clock buffers, and on-chip clock trees, typical high-speed DRAM and memory controllers utilize analog-type, digital-type or hybrid-type duty-cycle corrector (DCC) circuits [1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20]. The DCCs in DDR3, DDR4, LPDDR4, LPDDR5, and GDDR5 SDRAM applications performs duty-cycle error compensation of high-speed signal pins for a differential clock (CLK/CLKb), data signals (DQs), and a data strobe signal (DQS). The DCC is also employed as part of a delay-locked loop (DLL) for DDR3/DDR4 SDRAMs and is mounted at the front or rear end of the DLL circuit [8, 10, 17, 21, 22, 23].

Most DCCs used in DRAM applications utilize a small-swing to full-swing level shifter (= also known as a CML-to-CMOS level converter) [24, 25] to amplify the small-swing clock signal to full-swing CMOS level [1, 2, 6, 13, 20, 24, 25]. Generally, the conventional level shifter has a problem that is very vulnerable to process corner variation. [25] shows that the output duty cycle of the level shifter can be more than 10% distortion. Therefore, DCCs using a level shifter can cause large duty-cycle errors in the presence of process corner variation. A fundamental solution to the problem of DCC performance degradation caused by the level shifter is to remove the level shifter from the DCC structure.

In this Letter, a new process variation insensitive full-swing hybrid DCC for 6.8 Gbps memory I/O links is presented. The proposed DCC utilizes a new full-swing duty cycle adjuster (DCA) that can provide a full-swing output clock of 50% duty-cycle without using a level shifter that is vulnerable to process corner variation. The proposed DCA utilizes a new pseudo-differential feedback delay element (PFDE) with insensitivity to process corner and supply variation. Also, the proposed DCC adopts a hybrid architecture to achieve fast duty-cycle correction and lock information retention capability in power-down mode. Implemented in a 40-nm CMOS process, the proposed DCC achieves an operating frequency range of 0.8–3.4 GHz. The DCC dissipates 2.8 mW from a 1.0 V supply at 3.4 GHz and occupies an active area of only 0.0054 mm².

2. Proposed full-swing DCC architecture

Fig. 1 shows a block diagram of the proposed full-swing duty-cycle corrector (DCC). The on-chip clock buffer (CLK buffer) receives the small-swing differential external clock (CLK subtly/CLK subtly) and generates a full-swing differential clock (CLK subtly/CLK subtly) used as the input of the DCC. The proposed full-swing DCC consists of a full-swing duty cycle adjuster (DCA), a digital feedback block, and an analog feedback block.

The full-swing DCA includes two pseudo-differential feedback delay elements (PFDEs) connected in series. The
digital feedback block includes a comparator, a 7-bit up/down counter, a 7-bit digital-to-analog converter (DAC), and a counter controller. The analog feedback block includes a charge pump (CP). At the beginning of the DCC operation, the CP generates the $V_{ctrl}/V_{ctrlb}$ signal that is proportional to the duty-cycle error of the output CLKOUT/CLKOUTb clock. The first PFDE receives CLKIN/CLKINb as an input and uses $V_{ctrl}/V_{ctrlb}$ as a control signal to quickly correct the duty cycle of the CLKMID/CLKMIDb signal to 50% within a few tens of nanoseconds. The second PFDE slowly replaces the operation of the first PFDE using $V_{Dctrl}/V_{Dctrlb}$ signal, which is the output of the digital feedback block. The digital feedback block first converts the analog $V_{ctrl}/V_{ctrlb}$ signal to the digital code Q[6:0]/Qb[6:0] using a comparator and a 7-bit counter. Then, a 7-bit DAC generates the $V_{Dctrl}/V_{Dctrlb}$ signal, which is the control signal of the second PFDE, using the Q[6:0]/Qb[6:0] code.

The digital feedback block and the second PFDE are used to store duty-cycle correction information in power down mode to provide fast power mode transition of DCC. The digital feedback block operates at $1/16$ and $1/128$ of the input CLKIN frequency.

Fig. 2 shows a schematic of the proposed pseudo-differential feedback delay element, PFDE. This new PFDE receives a differential full-swing input (IN/INb) and generates a differential full-swing output (OUT/OUTb) signal with duty-cycle ratio corrected using the control voltage $V_{ctrl}/V_{ctrlb}$. The proposed PFDE consists of two stages (1st stage and 2nd stage), each stage consisting of two feedback delay elements (FDEs: FDE1 and FDE2) and one cross-coupled inverter. Each FDE contains two inverters (INV1 and INV2) and a positive feedback control unit (PFPU). The cross-coupled inverters contribute significantly to providing insensitive properties to supply variations [28, 29, 30]. As shown in the FDE1 of Fig. 2, the PFPU is a tri-state inverter having an analog signal $V_{ctrl}$ as a feedback strength control voltage. The gate inputs of the transistor $P_F$ and $N_F$ are connected to the output node $O$ of INV2 and the drain nodes of the transistor $P_C$ and $N_C$ are connected to the output node $Z$ of INV1. The PFPU can control the switching threshold voltage of INV1 using a positive feedback path that can adjust the feedback strength.

Fig. 3 shows the voltage transfer curve (VTC) simulation results of the proposed PFDE (i.e. INV1 of Fig. 2) showing hysteresis characteristics depending on the use of PFPU and the value of the control voltage $V_{ctrl}$.

As shown in Fig. 3(a), the switching threshold of INV1 (FDE1 of Fig. 2) becomes Point A when there is no PFPU block, and hysteresis characteristics are not seen when $V_{IN}$ increases or decreases. Fig. 3(b) shows the results when the PFPU is used with $V_{ctrl} = 0.5\, \text{V} (=V_{DD}/2)$. Due to the contention between the PFPU and INV1, the switching threshold of INV1 moves to point B when $V_{IN}$ changes from low-to-high and to point C when $V_{IN}$ changes from high-to-low [26]. This structure can be used as a delay element if the strength of the PFPU is adjusted to show symmetrical hysteresis characteristics (Point B and Point C) based on point A.

Fig. 3(c) and 3(d) show that the FDE structure can be used for duty-cycle correction when the $V_{ctrl}$ value is adjusted to create an hysteresis characteristic. Fig. 3(c) shows the case when $V_{ctrl} = 0.4\, \text{V}$. If $V_{IN}$ changes from low-to-high, the switching threshold of INV1 moves to point D. This is because the pull-up network ($P_F$ and $P_C$) of the PFPU is turn on when the initial value of the $O$ node is zero. In particular, as the feedback strength of the pull-up
network is further increased by increasing the Gate-Source voltage ($V_{GS}$) of $P_C$ by 0.1 V, the switching threshold point is shifted to point D, which is more right than point B of Fig. 2(b). This causes the falling time of the Z node to be delayed, thus delaying the rising time of the O node, resulting in an output clock (O node) with a reduced duty cycle. When $V_{IN}$ changes from high-to-low, the switching threshold of INV1 moves to point E. Point E is slightly on the right side of point C of Fig. 2(b). This is because the pull-down network $N_C$ is turned on by about 0.1 V weaker than in Fig. 2(b). This causes the rising time of the Z node to be reduced, thus resulting in an output clock (O node) with a reduced duty cycle.

Fig. 3(d) shows the case when $V_{ctrl} = 0.6$ V. In this case, the $P_C$ of the PFCU is slightly weakly turned on and the $N_C$ is slightly more turned on. When $V_{IN}$ changes from low-to-high, the switching threshold is shifted to point F. When $V_{IN}$ changes from high-to-low, the switching threshold is shifted to point G. As a result, the overall VTC moves to the right side, which can increase the duty cycle of the output O node. In the same way, the duty cycle of the Ob node of FDE2 can be increased or decreased by controlling $V_{ctrlb}$, which is symmetrical to $V_{ctrl}$.

We have confirmed that controlling the $V_{ctrl}$ (or $V_{ctrlb}$) voltage can change the switching threshold of the FDE. To use this as a DCC, it is now necessary to check the linearity characteristic. Fig. 4 shows the simulated linear characteristics of the proposed FDE according to the $V_{ctrl}$ voltage. In Fig. 4(a), when $V_{IN}$ changes from low-to-high, the pull-up network ($P_F$ and $P_C$) of the PFCU can be modeled with a current source ($I_{PC}$) and an equivalent resistor $R_{OP}$, where $R_{OP}$ is the on-resistance of $P_F$. Also, $C_Z$ is the total capacitance of the Z node. It can be seen that the $I_{PC}$ current decreases linearly as the $V_{ctrl}$ voltage increases. In Fig. 4(b), when $V_{IN}$ changes from high-to-low, the pull-down network ($N_F$ and $N_C$) of the PFCU can be modeled with a current source ($I_{NC}$) and an equivalent resistor $R_{ON}$, where $R_{ON}$ is the on-resistance of $N_F$. It can be seen that the $I_{NC}$ current increases linearly as the $V_{ctrl}$ voltage increases.

Fig. 5 shows the simulated linear duty cycle correction capability of the proposed PFDE shown in Fig. 2 according to the $V_{ctrl}$ voltage at 3.4 GHz. It can be seen that the output duty cycle ratio of the PFDE is linearly adjusted from about 30% to 70% when the $V_{ctrl}$ voltage varies from 0.4 V to 0.6 V.

3. Experimental results

The proposed full-swing DCC has been implemented in 40 nm 1.0 V CMOS process. Fig. 6 shows the chip layout of the proposed DCC core, which occupies an active area of only 0.0054 mm². Post-layout simulations have been completed to verify the performance of the proposed DCC. The DCC achieves a frequency range of 0.8–3.4 GHz and the duty correction range is about ±15% at 3.4 GHz.

Fig. 7 shows the locking process of the proposed full-swing DCC. The locking process can be divided into a duty cycle correcting period and a duty cycle tracking period. At about 150 $CLK_{IN}$ cycles after the DCC operation, the duty cycle of the output clock ($CLK_{OUT}/CLK_{OUTb}$) is corrected to 50% by the operation of the analog feedback block and the analog DCA shown in Fig. 2. The duty cycle tracking period is for digital DCA to replace the operation of the analog DCA. The operation of the digital DCA is controlled by the digital feedback block. The operation of the digital feedback block leads to the slow track mode through the fast track mode. At the beginning of the DCC operation, the digital feedback block operates at $CLK_{CONT} = 1/16 \times CLK_{IN}$ frequency in fast track mode and after 1024 $CLK_{IN}$ cycles, it is converted to slow track mode with $CLK_{CONT} = 1/128 \times CLK_{IN}$ frequency. This reduction of the operating frequency in the digital feedback block is to reduce dithering of the analog DCA control voltage ($V_{ctrl}$/
Vctrlb) and digital DCA control voltage (V_Dctrl/V_Dctrlb) and to improve jitter characteristics.

Fig. 8 shows the simulated duty-cycle correction operation of the proposed full-swing DCC at 3.4 GHz. When the DCC operation is off, a 3.4 GHz input clock with a duty-cycle of 40% enters the DCC block and outputs a clock with a duty-cycle of 40.23%. When the DCC operation is on, a 3.4 GHz input clock with a duty-cycle of 40% enters the DCC block and outputs a clock with a duty-cycle of 50.43%.

Fig. 9 shows the process corner simulation results of the proposed full-swing DCC when the input clock duty-cycle is changed from 35% to 65% (@3.4 GHz)

Fig. 10 shows the simulated peak-to-peak (p-p) output clock jitter of the proposed DCC at 3.4 GHz. When there is no supply noise, the proposed DCC achieves a p-p jitter of only 1.91 ps. Even if artificially injecting 175 MHz supply noise of 100 mV, the p-p output clock jitter increases to 12.8 ps, but still performs stable DCC operation.

Table I shows a comparison between the proposed full-swing DCC and other state-of-the-art DCCs for high-speed memory interface. Among the DCCs in Table I, the proposed DCC has the highest power efficiency and the smallest chip area while providing a wide operating frequency range.

4. Conclusion

A new process variation insensitive full-swing DCC for high-speed memory I/O links is presented. The proposed full-swing DCC is based on the new pseudo-differential
FDE and eliminates the use of level shifters to obtain process insensitive characteristics. Implemented in a 40-nm CMOS process, the proposed DCC achieves high power efficiency and small chip area while providing a wide operating frequency range. The proposed DCC is suitable for use in next-generation DRAM applications such as 6.4 Gbps/pin DDR5.

Acknowledgments

This research was funded and conducted under “the Competency Development Program for Industry Specialists” of the Korean Ministry of Trade, Industry and Energy (MOTIE), operated by Korea Institute for Advancement of Technology (KIAT). (No. N0001883, HRD program for N0001883). This work was also supported by National Research Foundation of Korea (NRF 2019R1A2C1010017). The EDA tools were supported by IDEC.

References