Fabrication of embossed capacitive micromachined ultrasonic transducers using sacrificial release process

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Abstract: An embossed capacitive micromachined ultrasonic transducer (CMUT) is a device with embossed membrane that works in the collapse mode to improve output pressure in transmission. In this paper, a six-mask sacrificial release process is proposed for fabricating embossed CMUT arrays. Based on this process, the embossed pattern CMUTs were firstly fabricated. By using of electroplating methods, annular embossed patterns made of nickel were grown on the full top electrodes of CMUTs. The dimensions of the embossed pattern were about 3.0 μm in width and 1.4 μm in height. The resonant frequencies of the embossed CMUT array were 6.4 MHz and 8.7 MHz when the device worked in the conventional and the collapse mode, respectively.

Keywords: embossed capacitive micromachined ultrasonic transducer, nickel electroplating, sacrificial release process

Classification: Micro- or nano-electromechanical systems

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1 Introduction

Capacitive micromachined ultrasonic transducer (CMUT) is a type of ultrasonic transducer based on electrostatic principle and was invented around 1990s [1, 2]. CMUTs are superior to piezoelectric ultrasonic transducers because of their acoustic impedances are more matched to medium. As the acoustic impedance of CMUTs is low and can be adjusted [3], CMUTs achieve a broader bandwidth in both airborne and immersion applications as compared with piezoelectric ultrasonic transducers. In addition, CMUTs also own other merits, such as higher working frequencies, Complementary Metal-Oxide-Semiconductor (CMOS)-compatible fabrication processes, and easier to fabricate large arrays [4]. These features make CMUTs as promising alternative ultrasonic transducers in the field of medical ultrasonic imaging, which demands a high integrated and wide bandwidth ultrasonic probe. In the past years, CMUTs have been utilized in medical areas, such as ultrasonic imaging [5, 6] and therapeutic applications [7, 8]. Recently, owing to the features of wide bandwidth and fabricated by micro-electro-mechanical systems (MEMS) technique, CMUTs have also been used in photoacoustic imaging and achieved high quality images [9, 10].

Comparing with piezoelectric transducers, the lower output pressure of CMUTs limits their further developments in medical imaging. A higher acoustic pressure in ultrasonic imaging increases the detection depth and signal-to-noise ratio of images. Recently, a method of forming an embossed membrane on a collapse mode CMUT was proposed for improving the output pressure in transmission [11]. The structure of a CMUT with embossed membrane is described in Fig. 1. When the applied DC bias voltage is higher than the pull-in voltage, the membrane will be collapsed and partially pressed to the insulator due to the high electric field force inside the cavity. In this case, the CMUT works in the collapse mode in which the center portion of the membrane contacts on the insulator in operation. The annular vibrating membrane between the rim and contacted portion acts as the source of ultrasonic waves. An annular ring, called as embossed pattern, is designed on the top electrode, which fully covers the circular membrane to keep equal effective density of the composited materials beneath the embossed pattern. It was revealed that strain energy of the vibrating membrane can be enhanced with the embossed pattern and the optimum pattern position is the vibrating center of the membrane. By tuning DC bias voltage, the vibrating center of membrane can be adjusted to the position of the embossed pattern. In this way, the output pressure can be increased because the maximum vibration amplitude of vibrating membrane is enlarged. The material of the embossed pattern can be dielectric or metal and it was found that the material with a higher density can generate more output pressure.

In this article, a six-mask sacrificial release process to form an embossed pattern on the membrane of CMUT is proposed. This process is compatible with the traditional CMUTs fabrication technology [12, 13] and we are the first research group to fabricate the embossed CMUT arrays based on this process.

2 CMUT design parameters

An annular embossed pattern made of nickel was designed on the full top electrode

Fig. 1. Design of an embossed CMUT

of CMUT. A two-dimensional axisymmetric finite element analysis (FEA) model representing a CMUT cell in transmission mode was developed to initially design dimensions of the embossed CMUT arrays and to investigate the characteristics of the CMUT such as, pull-in voltage and resonant frequency of the device in air. This model was built with COMSOL Multiphysics 4.4 (COMSOL Inc., Stockholm, Sweden), as shown in Fig. 2. In this model, the CMUT cell was coupled with surrounding medium of air represented by a cylindrical waveguide with height larger than one wavelength of acoustic wave in air and width equal to half of the CMUT cell pitch. To eliminate wave reflection, an absorbing boundary was applied on the top of the waveguide. The CMUT and waveguide were governed by the electromechanics (*emi*) physics, which was coupled with the pressure acoustic (*acpr*) physics that governed the waveguide [11]. Stationary study was used in simulation and the pull-in voltage was calculated by steeply increasing the DC bias voltage applied on the CMUT just until the solution on the verge of divergence. In this design, the resonant frequency of CMUT was calculated by finding the maximum output pressure over frequencies with averaging the surface pressure along the interface between embossed membrane and medium. To avoid divergence, a penalty/barrier method was introduced to handle the contact of membrane and insulator caused by the DC bias voltage above the pull-in voltage [14]. The material of the membrane is low-stress silicon nitride with the $E \approx 220$ GPa, $\sigma \approx 0.263$, and $\rho \approx 3270$ kg/m³.

Assisted with the FEA model, the parameters of the embossed CMUTs were determined and listed in Table I. The estimated pull-in voltage was 80 V and the resonant frequencies was about 6.7 MHz and 8.5 MHz in conventional and collapse regions, respectively.

3 Fabrication process

In consideration of the device structure, a six-mask process with photolithography was proposed for fabrication.

3.1 Insulator and sacrificial layer deposition

An *N*-type highly doped (resistivity: 0.1 to 1 ohm-cm) 4-inch silicon wafer with the crystal orientation of $\langle 100 \rangle$ acted as the substrate and common bottom electrode for device. Firstly, a 150 nm thermal SiO₂ layer was grown by using a dry oxidation process (SJ-CA1200-D4, SJ, Taiwan), then a 150 nm low stress silicon nitride layer was deposited on the oxidation layer by low pressure chemical vapor deposition

Fig. 2. An FEA model for CMUT design (Not drawn in scale)

Table I. Design parameters of embossed CMUT.

Dimension	(μm)
Membrane (Si_3N_4) radius	20
Membrane (Si_3N_4) thickness	0.65
Gap height	0.30
Insulator1 (SiO_2) thickness	0.15
Insulator2 (Si_3N_4) thickness	0.15
Top electrode (Gold) radius	20
Top electrode (Gold) thickness	0.18
Chromium adhesion layer thickness	0.02
Embossed pattern (Nickel) width	3.0
Embossed pattern (Nickel) height	1.5
Embossed pattern inner radius	10.5
Embossed pattern outer radius	13.5

(LPCVD) process (SJ-10301001-1, SJ, Taiwan). These two layers acted as the combined insulation layer and the nitride layer also acted as an etch stop in the later process of releasing sacrificial layer. After the formation of insulation layer, a 300 nm poly-silicon layer was grown upon the insulator by LPCVD.

3.2 CMUT definition

The shape of the CMUT, including cavity and release channels were patterned on the poly-silicon layer with the Mask #1 (Fig. 7(a) in Appendix) photolithography. Before coating the positive photoresist on the wafer, an hexamethyldisilazane (HMDS) process was applied to promote good photoresist-to-wafer adhesions. A thickness of 1.6 μm photoresist was coated on the wafer by a spin coater (NC990907-03, DA-HE Technology Co., Taiwan), and then processed with a soft baking (90 $^{\circ}\text{C}$, 90 s). The mask alignment and exposure were executed on a double side mask aligner (AG1000-4D-D-S-M-V, M & R Nano Technology Co., Ltd., Taiwan). After the development and hard baking processes, the wafer was etched

by a reactive ion etching (RIE) process (RIE-10N, SAMCO, Japan) to form the shapes of CMUT cells.

3.3 Membrane deposition and forming etch holes

A thickness of 650 nm low stress silicon nitride layer was deposited as the membrane and structure layer by LPCVD. Then four etch holes at the end of release channels were defined on the silicon nitride layer by the Mask #2 (Fig. 7(b) in Appendix) photolithography. Four etch holes of 2 μm in diameter were designed surrounding one CMUT cell to accelerate the sacrificial release process. After the photolithography, the silicon nitride inside the etch holes were fully removed by a RIE process. After this procedure, the poly-silicon underneath the low stress silicon nitride layer was exposed via the etched holes.

3.4 Releasing sacrificial layer and sealing etch holes

Potassium hydroxide (KOH) was the etchant for releasing sacrificial layer of poly-silicon. Although the etch rate of KOH grows with temperature, increasing temperature for fast etching is not preferred as the selectivity become worse. In addition, during poly-silicon etching, hydrogen (H_2) is generated in solution. Therefore, increasing the reaction temperature, intense bubbles inside the cavities may break the thin membrane during releasing process. As referred the etching rate of KOH concentration from reference [15], the wafer was immersed in a 22.5 wt% KOH solution at room temperature (20 $^{\circ}\text{C}$) to release the sacrificial layer. It took about 56 hours for fully etching away the poly-silicon layer via the etch holes. Potassium ion (K^+) is an extremely fast-diffusing alkali metal ion and a serious contaminant for Metal-Oxide-Semiconductor (MOS) devices. Therefore a decontamination procedure referred from Stanford Nanofabrication Facility [16] was carried out to prevent facility contamination in the subsequent process.

The CMUT cavity should be sealed for both air and immersion applications to reduce the squeeze loss inside the cavity. In this design, the cavity was then sealed at the etch holes by depositing a silicon nitride layer with thickness of 1.2 μm using a process of plasma enhanced chemical vapor deposition (PECVD) (PD-220N, SAMCO, Japan).

3.5 Thinning membrane

In the previous process, the whole wafer was coated with a 1.2 μm PECVD silicon nitride layer. The membrane should be thinned to its initial design of 650 nm by removing this additional silicon nitride layer. The silicon nitride near the sealed hole was preserved in thinning process to prevent damages to the sealing. After an HMDS process, the wafer was coated with a 2 μm thickness positive photoresist and exposed by the Mask #3 (Fig. 7(c) in Appendix). The thinning process was carried out by a RIE process.

3.6 Bottom pad definition and metalization

After the previous processes, the highly doped wafer was coated with multiple non-conductive materials. Prior to the metalization process, it is necessary to form pathways to the silicon substrate. In this design, a 100 $\mu\text{m} \times 100 \mu\text{m}$ pad for bottom

electrode of each CMUT array was defined. The wafer coated with a thickness of 2 μm positive photoresist was exposed by the mask aligner with the Mask #4 (Fig. 7(d) in Appendix) and dry etched by RIE. After this process, all non-conductive materials in the pad area for bottom electrode were removed.

The subsequent procedure was the metalization on the whole wafer. Although aluminum is commonly used in CMUT metalization, in the subsequent procedure, the embossed pattern was formed on the metal layer with electroplating methods in heated acid solutions. If the electrode metal were aluminum, it would be easily oxidized in electroplating. Gold, owing to good chemical and mechanical properties, was chosen as the metalization material in this design. A stacked metal layer consist of 20 nm chromium and 180 nm gold was deposited in sequence by an electron beam evaporator (ULVAC, Japan). The thin chromium layer acted as an adhesion between gold and the substrate materials, including silicon nitride and silicon.

3.7 Forming nickel embossed pattern

In accordance with reference [11], a higher density embossed pattern achieved better performance. In this design, the embossed pattern was made of nickel and formed on top electrode by electroplating methods. As positive photoresist was used in photolithography, the thickness of photoresist should be higher than the height of the embossed pattern. The wafer was coated with a 2 μm thick positive photoresist and exposed by the mask aligner with the Mask #5 (Fig. 7(e) in Appendix), which defined the widths and positions of embossed patterns.

The electroplating was carried out by using the Watts nickel plating baths [17]. A recipe of $\text{NiSO}_4 \cdot 6\text{H}_2\text{O} : \text{NiCl}_2 \cdot 6\text{H}_2\text{O} : \text{H}_3\text{BO}_3 : \text{H}_2\text{O} = 676 : 114 : 96 : 2400$ (g) was used in plating. The temperature of bath was controlled at 48 $^\circ\text{C}$ and a DC constant current was set to 20 mA. The plating time was 120 seconds and the estimated thickness of nickel layer was about 1.5 μm .

The nickel electroplating setup was shown in Fig. 3. After plating, the wafer was cleaned by deionized water and acetone in sequence to remove the photoresist around the embossed pattern.

Fig. 3. Nickel electroplating setup. A pure nickel plate acted as the anode and the metalized wafer acted as the cathode, each of them was placed in a Teflon holder, respectively.

3.8 Top electrode definition

The last Mask #6 (Fig. 7(f) in Appendix) was used to define the full top electrode, cell interconnections, and bonding pads (top and bottom electrodes) for CMUT array on the metal layer. The width for interconnection was designed as 4 μm and the dimension of bonding pad was 100 μm $\times$ 100 μm . The wafer was coated with a 1.2 μm thick positive photoresist and exposed by the mask aligner.

A solution with the recipe of $\text{I}_2 : \text{KI} : \text{H}_2\text{O} = 65 : 113 : 200$ (g) was used to etch gold. After the gold etching, the adhesion material of chromium was etched by the chromium etchant of CR-7. When all the metals in the exposed region were fully etched away, top electrodes, bottom electrodes, interconnections and bonding pads were formed. After striping the photoresist, the embossed CMUTs were fabricated, shown in Fig. 4, which was observed by a microscope (BX63, Olympus, Japan).

4 Measurement and discussion

4.1 Measurement results

After the fabrication, the embossed CMUTs were measured by the FIB/SEM system. Fig. 5 shows that the width of the nickel pattern was about 3 μm , which was similar to the design parameter. Please note that the vertical measurement values (875 nm and 1.38 μm) in this figure should be adjusted manually because the measuring angle was 52 degree. The corrected value of the height of embossed pattern was about 1.42 μm , which was slightly smaller than the design parameter of 1.5 μm . The corrected thickness of the embossed area, including membrane, electrode and embossed pattern was 2.24 μm , which was also close to the sum of these design parameters.

The measurement of electrical input impedance in air is used to characterize the resonant frequency of CMUT because it can be represented by the Masons two ports equivalent circuit model [3]. The electrical port contains the clamped capacitance of device and the mechanical port consists of the spring softening capacitance, the membrane impedance and coupling medium impedance. The membrane impedance is generally a combination RLC circuits and the medium impedance resembles a resistor. Whenever a CMUT operating in air, the membrane impedance at resonance is comparable to the medium impedance. As a result, the equivalent circuit behaves as an RLC resonant circuit and the maximum real part of impedance occurs when the membrane resonant. The input impedance of the embossed CMUTs was measured by a network/spectrum/impedance analyzer (4395A, Agilent Technologies Inc., United States) and a programmable DC power supply (HSPY-400-01, Beijing HanShengPuYuan Technology Co., Ltd., China). Prior to measurement, the analyzer was properly calibrated. The DC bias was provided by the DC power and a small AC excitation was applied from the analyzer while sweeping the frequency. To measure the pull-in voltage, the resonant frequency was observed with increasing the DC bias voltage by 1 V steps. The pull-in voltage was determined by a sudden resonant frequency shift-up when the membrane collapsed. The pull-in voltage of the embossed CMUT array was about 65 V, which was lower than the simulated value. One possible reason is that the gap

Fig. 4. Embossed CMUTs observed by an optical microscope.

Fig. 5. Dimensions of the embossed pattern measured by FIB/SEM.

height was less than design due to the surface roughness on both the gap side of the silicon nitride layers after sacrificial layer releasing [15].

Fig. 6 is the real and imaginary parts of input impedances of the embossed CMUT array under different DC bias voltages. If the bias voltage was lower than the pull-in voltage, the CMUTs worked in the conventional mode, in which the resonant frequency was 6.4 MHz when biased at 40 V. When applying a DC voltage above the pull-in voltage, the center of membrane is pulled down and contacted to the insulator all the time in operation. In this scenario, only the annular portion between the rim and contacted area contributes the vibration. Therefore, there is a resonant frequency upshift when the CMUT goes into collapse mode from conventional mode. It was observed that the resonant frequency of the embossed CMUT array shifted to 8.7 MHz when applying a DC bias voltage of 90 V, which indicated that the embossed membranes were collapsed. The resonant frequencies in both conventional and collapse modes were close to the FEA simulations. The higher resonant frequency of collapse mode in measurement can be attributed to the less gap height of device. The collapsed radius of the membrane was larger than that in simulation and therefore the width of the annular vibrating membrane was smaller.

Fig. 6. Input impedances of the embossed CMUT array in conventional and collapse modes.

4.2 Discussion

In this fabrication, the material of the embossed pattern was nickel in accordance with reference [11], which revealed that a higher density material can achieve more improvement on output pressure. The nickel patterns were formed by electroplating methods because the deposition rate is relative high. Comparing with sputtering or thermal evaporation, electroplating is an efficient and economical method to deposit a nickel layer with the thickness larger than 1 μm .

The FIB/SEM measurement on the fabricated device showed that the dimension of the nickel pattern was close to the design parameters. However, it was difficult to accurately control the dimension of the designed pattern in fabrication. Firstly, the patterns were defined by the #5 Mask, in which only the annular areas for the embossed patterns were designed as the clear fields because of using positive photoresist. In this photolithography, the exposure time and light intensity should be carefully controlled to ensure that the sizes of all the exposure areas on the wafer were close to the patterns in the mask. Secondly, the developing area defined the pattern area and the residual photoresist constrained the maximum height for the pattern. The nickel was grown inside the non-photoresist area by electroplating methods. The operating conditions, such as the DC current, time and temperature should be controlled precisely. In the process of electroplating, an optical microscope was used for observing the progress. However, the height of the pattern could not be measured by the optical microscope. With the assistance of FIB/SEM, it was found that the height of the deposited embossed pattern was slightly less than the design parameter.

The pull-in voltage and resonant frequency of the CMUT array were measured by an impedance analyzer. With increasing DC bias voltage, it was found that the membrane collapsed and the resonant frequency shifted when the DC bias was higher than the pull-in voltage. The optical and electrical measurement results showed that the embossed CMUTs were fabricated successfully.

5 Conclusion

In this work, a six-mask sacrificial release process for forming embossed CMUTs was proposed and applied for fabrication. This process is compatible with the current CMUT fabrication methods. With electroplating methods, the annular nickel patterns were fabricated on the gold electrodes successfully. The FIB/

SEM measurement showed that the dimensions of the embossed pattern were close to the design parameters. Furthermore, the resonant frequencies below and above pull-in voltage were measured. It showed that the embossed CMUT can work properly in both conventional and collapse modes by applying different DC bias voltages. These measurements indicated that the embossed CMUTs were fabricated successfully based on the proposed process.

6 Appendix

6.1 Sketches of CMUTs in fabrication process

In accordance with the fabrication process of embossed CMUTs, six Masks were designed. Fig. 7 demonstrates the sketches of CMUTs from Mask #1 to Mask #6, respectively.

Fig. 7. Sketches of Mask design in each process. (a) to (f) represents Mask #1 to Mask #6, respectively. Please note that (d) is not in scale with the others.

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