LETTER

Eye-open monitor using two-dimensional counter value profile

Kyung-Sub Son¹, Yong-Hwan Moon¹, Sanghun Baek¹, Namyong Kim¹, Taek-Joon An¹, and Jin-Ku Kang^{1a)}

Abstract A simple eye-opening monitor (EOM) system based on two dimensional (2-D) counter-value profile is designed. The proposed EOM can be applied to adaptive equalizer coefficient control for better bit error rate (BER) performance in the high-speed serial interface. Input data is sampled 2048 times with 32 different clock phases on 32 different decision threshold amplitudes to the clocked comparator and the sampled outputs of '1' or '0' are recorded in the designated counter. The counter values at each phase and decision threshold amplitude are compared with a reference of 1024 for eye-opening monitor. The estimated eye-diagram is displayed on the monitor. Through the estimated eye-diagram, the optimal sampling timing can also be determined. The chip for sampling data and gathering the counter value has been designed through 180-nm CMOS process and 86 mW including I/O block is consumed on 2 Gb/s data rate.

Keywords: eye-open monitor, eye-diagram, optimal sampling point

Classification: Integrated circuits

1. Introduction

In high-speed serial interfaces, the signal integrity is degraded by jitter and inter symbol interference (ISI) caused from the channel. In the receiver side filters such as continuous-time linear equalizer (CTLE) or decision feedback equalizer (DFE) are inserted before the clock and data recovery (CDR). For adjusting the coefficient of filters, feedback processes, such as least mean square (LMS) or bit-error-rate (BER) metrics feedback, are needed [1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30].

By minimizing the mean square error (MSE), the sign-sign least-mean-square (SS-LMS) algorithm adjusts the coefficients of filters [1, 2, 3, 4]. Adaptation loop by SS-LMS algorithm is done either in voltage domain or time domain.

Utilizing BER metrics for filter coefficient update and sampling clock phase update costs a longer update period and complex hardware, which is usually implemented in off chip processing hardware. Therefore efficient algorithms are necessary for BER metrics approach. The hill-climbing algorithms from estimated BER for optimal filter coefficients are studied [5, 6]. The outputs from two different samplers are compared after BER metrics feedback by controlling decision threshold voltage and clock phases.

An eye-opening monitor (EOM) is a way to measure the data. Thus after processing EOM information by a certain algorithm, filter's coefficient and clock timing can

Fig. 1. Receiver circuit with an EOM.

also be adjusted [7, 8, 9, 10, 11]. The typical block diagram for EOM feedback in the receiver is shown in Fig. 1. Histogram approach for monitoring the contour and dispersion of the eye-diagram is done by voltage amplitude control [7] and clock phase control [8]. In ref. [9], both clock phase and voltage amplitude control, which is called two dimensional (2-D) eye-monitoring, are applied with an eye-opening mask. EOM combined with BER metrics feedback for finding the optimal data sampling point was investigated in [10]. For more accurate BER estimation, the more data should be processed. As a result the longer time and larger silicon area are required. A fast and on-chip BER-based EOM was possible by stochastic eye-opening monitor [11]. The approach detects the BER-related one-sigma eye contour for estimating the optimal eye-opening.

This letter suggests a simple approach for EOM from counter values obtained through 2-D data sampling. The input data is sampled through a clocked comparator on different decision threshold amplitudes (32-levels) and different sampling clock phases (32-phases). In this scheme, only one clocked comparator for the sampler is needed. The output of the sampler is either '1' or '0'. At each amplitude and phase, input data are sampled 2048 times and the sampled outputs are recorded in the counter. The counter values at each phase and decision threshold amplitude are compared with a reference of 1024 for eye-opening monitor. The estimated eye-diagram is displayed on the monitor. The eye-diagram can be utilized for adjusting the equalizer coefficient and the sampling clock phase in the CDR. BER metrics are easily added to the proposed EOM if necessary.

2. Proposed architecture

A. Operation Principle

Fig. 2 shows the block diagram for the proposed EOM. On-chip blocks are a clock and data recovery (CDR), a clocked comparator, a digital-to-time converter (DTC) for phase step control, a digital-to-analog converter (DAC) for decision threshold amplitude step control and 11-bit coun-

¹Dept. of Electrical Engineering, Inha University, 100 Inha-ro, Nam-gu, Incheon 402-751, Republic of Korea

a) jkang@inha.ac.kr

DOI: 10.1587/elex.16.20190601

Received September 27, 2019

Accepted October 2, 2019

Published October 17, 2019

Copyedited November 12, 2019

Fig. 2. Block diagram of the proposed EOM.

ter. Digital processing for the data eye estimation from the counter value is done in FPGA. DTC and DAC steps are controlled by 5-bit signals and both have 32 steps. A personal computer (PC) is for controlling the whole system. The output from the clocked comparator is obtained at each sampling point (phase and decision threshold amplitude). The comparator outputs either '1' or '0'. Input data are sampled 2048 times at each sampling point and the output of the comparator is recorded in the 11-bit counter. After storing all counter outputs at 32 by 32 sampling point, the digital processing block in FPGA estimates the data eye by comparing the counter value at each sampling point.

Fig. 3. (a) Clocked comparator, (b) relationship between data eye and sampling points (the dot is the optimal sampling point), and (c) counter output value ($OUT_{i,j}$) profile with ϕ_0 and ϕ_{15} while the decision threshold amplitude (A_i) sweeps.

Fig. 3(a) shows the sampler circuit, which is a clocked comparator. The clocked comparator outputs at the sampling clock phase (ϕ_j) by comparing input data level with the decision threshold amplitude (A_i). Fig. 3(b) illustrates the relationship between data eye and the sampling points (A_i, ϕ_j). For the best BER, the sampling clock of ϕ_{15} should be placed in the middle of the data eye.

The sampling point at the clocked comparator is determined by DAC and DTC. The rising edge of input data is synchronized with the sampling clock, ϕ_0 . As shown in Fig. 3(b), if data's rising edge is near at ϕ_0 , the data eye is almost closed. And if data's rising edge is near at ϕ_{15} the data eye is open most widely. Assuming data transition probability is the same, the counter output is near 1024 in the center region of the data eye. In opposite case, where the sampling phase is near the data edge, the counter output is much less

than 1024. Fig. 3(c) shows two different counter output profiles at ϕ_0 and ϕ_{15} as the decision threshold amplitude (A_i) sweeps from the minimum to the maximum. With ϕ_{15} the average counter output is near 1024 for most of the amplitude levels. With ϕ_0 the counter value output is decreased sharply from the middle of decision threshold amplitude. After obtaining all counter values from all sampling points, data eye opening can be estimated by comparing the counter values at each point with a reference value of 1024. The relative difference from 1024 at each sampling point gives the contour of data eye that can be displayed in the monitor. B. Circuit Design

Fig. 4 shows the circuit diagram of the clocked comparator. It captures the data at the designated clock phase and the decision threshold amplitude. As stated before, the sampling clock phase (ϕ_j) and the decision threshold amplitude (A_i) are controlled by DTC and DAC, respectively. The DTC is controlled by 5-to-32 thermometer code.

Fig. 5(a) shows a DTC circuit which is a phase rotator generating 32 phases from 4 clock phases. The DTC first selects two phases (I, Q) from 4 clock phases and interpolates the phases to finer 8 different phases. Thus the sampling clock phase is controlled by 5-bit. In order to reduce an offset during the phase selection switching, a small current source

Fig. 4. Circuit diagram of the clocked comparator.

Fig. 5. (a) DTC, (b) DAC.

((I_{offset}) is used. Fig. 5(b) illustrates a current-mode 5-bit DAC. The decision threshold level is determined by the amount of the selected drain current (I_{DAC}). The DAC is also controlled by 5-to-32 thermometer code.

C. Simulation Results

First, the proposed EOM was simulated using an input data. Fig. 6 shows an estimated eye diagram through the proposed scheme. The brighter patterns appear where the counter output value is near 1024. When the counter output is lower than 1024, the darker pattern is illustrated. The lower the counter value is, the darker the pattern is. The optimal sampling point is derived and it is where the eye has the maximum height and width and the point is given inside eye opening area.

Fig. 7 shows two different counter output values at Φ_0 and Φ_{15} by sweeping the decision threshold amplitude from the lowest level to the maximum level. Fig. 7(a) is the counter output profile sampled at Φ_{15} , which is positioned near the data center. As the decision threshold is moved from the center level, the counter output stays at almost same level until the limit levels. Fig. 7(b) is the counter output profile sampled at Φ_0 , which is positioned near the data edge. As the decision threshold is moved from the center level, the counter output drops very sharply. Therefore the counter values obtained through sweeping the decision threshold amplitude at each sampling points gives an estimated eye-opening. Fig. 8 shows two different eye diagram output from two different input jitter condition. As shown, the more input jitter results in less eye-opening.

3. Measured results

The chip for the proposed EOM has been designed and fabricated using a 180-nm CMOS process. The chip in-

Fig. 6. Eye diagram generated using an input data. The dot shows an optimal sampling point.

Fig. 7. (a) Counter output profile obtained at 15th clock phase, (b) at 0th clock phase by sweeping the decision threshold amplitude.

Fig. 8. Eye diagrams obtained from two different jitter conditions (a) high input jitter case (b) lower input jitter case. (left: input data eye, right: EOM generated data eye).

cludes the sampler (clocked comparator), DTC/DAC, CDR, and the counter. Fig. 9 shows the chip photo and a detailed layout. All circuit blocks are implemented with full-custom-based circuit design methodology and the layout is done with Cadence tools. Loop filters of the CDR are placed off the chip. Current-mode-logic (CML) divider is used with an input buffer for providing the reference clock to the CDR. The CML-to-CMOS (C2C) level converter is inserted between phase rotator and sampler (clocked comparator) since the sampler needs a clock signal with a full CMOS level. The chip area is $2000\mu\text{m} \times 500\mu\text{m}$ and the power consumption is measured as 86 mW including I/O buffers at 2 Gb/s data rate.

Fig. 10 illustrates the test setup. The device-under-test (DUT) is the chip and a reference clock and input data are provided by a pulse generator. The PC commands the testing conditions to make the FPGA generate the proper control signals and carry the estimated data eye to the monitor. The recovered clock and data with sampling point information (clock phase and voltage level) can be measured with an oscilloscope.

Fig. 9. Chip microphotograph and detailed layout.

Fig. 10. Chip microphotograph.

Fig. 11 shows measurement results of DTC and DAC, respectively. The normalized phase of sampling clock on corresponding digital codes is given in Fig. 11(a). A linear phase shift on digital code change is shown between digital code of 6 and 25. Therefore actual phase steps controllable are 20 instead of 32. This is due to the minimum current for activating the phase interpolation. The LSB of DTC is 48 ps, INL is ± 0.20 LSB, and DNL is ± 0.80 LSB. Fig. 11(b) shows the normalized decision threshold amplitudes on digital codes. The amplitude level between 0.6 V and 1.8 V is converted to 30 different levels upon 5 bit digital code. The measured LSB of DAC is 40 mV, INL is ± 0.13 LSB, and DNL is ± 0.87 LSB.

Fig. 11. Normalized sampling phase and amplitude from (a) measured DTC and (b) DAC.

The measured EOM from the input signal is shown in Fig. 12. The data rate of applied input signal is 2 Gb/s with 400 mV peak-to-peak swing. An estimated data eye on the monitor is in Fig. 12(b). There is a brightness difference depending on the counter value compared to 1024. In the data edge region, the counter value is low, in which it appears as a darker region. In the center of data eye, the counter value is high, where it is illustrated as a bright region. The brightest area is where the counter value is 1024. The dotted line stands for the border line of estimated data eye opening by filtering the counter value profile and the center dot is the optimal sampling point.

Fig. 12. (a) Typical eye diagram measured with oscilloscope, (b) estimated data eye in the monitor (dotted line: estimated eye opening, dot: optimal sampling point).

Fig. 13. Input signals from different jitter conditions and their EOM's. Case of input signal (a) with a minimum jitter, (b) with a medium jitter, and (c) with a maximum jitter. (dotted line: estimated eye opening, dot: optimal sampling point).

Fig. 13 shows three different EOM profile on different input jitter conditions. More jitter in input data means a narrow data eye width on the monitor. The same maximum height on different jitter condition comes from the limiting amplifier in the input buffer stage.

Table I shows the performance summary and comparison with other works. Ref. [7] and [8] has only one-dimensional analysis by either phase or voltage amplitude change only. In ref. [9, 10, 11], two dimensional eye-open

Table I. Performance summary

	[7]	[8]	[9]	[10]	[11]	This work
Process	90 nm CMOS	180 nm CMOS	130 nm CMOS	180 nm SiGe	40 nm CMOS	180 nm CMOS
Data-rate	10 Gb/s	2 Gb/s	12.5 Gb/s	40 Gb/s	28 Gb/s	2.0 Gb/s
Eye Dimension	1-D (x)	1-D (y)	2-D	2-D	2-D	2-D
Algorithm	-	-	MER ¹⁾	CMER ²⁾	SS-EOM ³⁾	Counter Profile
Sampling Point adjustment (Amplitude)	Yes	No	Yes	Yes	Yes	Yes
Sampling Point adjustment (Phase)	No	Yes	Yes	Yes	Yes	Yes
Power Consumption	11 mW	110 mW	330 mW	1.6 W	43.9 mW	86 mW

1) Mask Error Rate (MER)

2) Code Mismatch Error Rate (CMER)

3) Stochastic Sigma-tracking EOM

monitoring is applied. However, these EOM combined with BER metrics requires complex algorithms with a larger hardware, or a higher power consumption with SiGe process. This work suggests a simple 2-D EOM system by only processing the counter value profile. The data rate and power consumption can be optimized with a better process technology.

4. Conclusion

A simple 2-D EOM based on counter-value profile is suggested. Input data is sampled 2048 times with 32 different clock phases on 32 different decision threshold amplitudes to the comparator. The counter value at each phase and each decision threshold amplitude is processed for eye-opening monitor. The estimated eye-diagram is displayed on the monitor. Through the estimated eye-diagram the optimal sampling timing can also be determined. It can be used with an adaptive equalizer for better BER performance.

Acknowledgments

This research was supported by Inha University. The authors also thank IDEC for CAD tool support.

References

- [1] F. Zhong, *et al.*: “A 1.0625~14.025 Gb/s multi-media transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS,” *IEEE J. Solid-State Circuits* **46** (2011) 3126 (DOI: [10.1109/JSSC.2011.2168871](https://doi.org/10.1109/JSSC.2011.2168871)).
- [2] V. Balan, *et al.*: “A 15–22 Gbps serial link in 28 nm CMOS with direct DFE,” *IEEE J. Solid-State Circuits* **49** (2014) 3104 (DOI: [10.1109/JSSC.2014.2349992](https://doi.org/10.1109/JSSC.2014.2349992)).
- [3] R. Payne, *et al.*: “A 6.25-Gb/s binary transceiver in 0.13- μ m CMOS for serial data transmission across high loss legacy backplane channels,” *IEEE J. Solid-State Circuits* **40** (2005) 2646 (DOI: [10.1109/JSSC.2005.856583](https://doi.org/10.1109/JSSC.2005.856583)).
- [4] J. Savoj, *et al.*: “A low-power 0.5–6.6 Gb/s wireline transceiver embedded in low-cost 28 nm FPGAs,” *IEEE J. Solid-State Circuits* **48** (2013) 2582 (DOI: [10.1109/JSSC.2013.2274824](https://doi.org/10.1109/JSSC.2013.2274824)).
- [5] E.-H. Chen, *et al.*: “Near-optimal equalizer and timing adaptation for I/O links using a BER-based metric,” *IEEE J. Solid-State Circuits* **43** (2008) 2144 (DOI: [10.1109/JSSC.2008.2001871](https://doi.org/10.1109/JSSC.2008.2001871)).
- [6] S. Son, *et al.*: “A 2.3-mW, 5-Gb/s low-power decision-feedback equalizer receiver front-end and its two-step, minimum bit-error-rate adaptation algorithm,” *IEEE J. Solid-State Circuits* **48** (2013) 2693 (DOI: [10.1109/JSSC.2013.2274904](https://doi.org/10.1109/JSSC.2013.2274904)).
- [7] C.-K. Seong, *et al.*: “A 10-Gb/s adaptive look-ahead decision feedback equalizer with an eye-opening monitor,” *IEEE Trans. Circuits Syst. II, Exp. Briefs* **59** (2012) 209 (DOI: [10.1109/TCSII.2012.2186366](https://doi.org/10.1109/TCSII.2012.2186366)).
- [8] F. Gerfers, *et al.*: “A 0.2–2 Gb/s 6x OSR receiver using a digitally self-adaptive equalizer,” *IEEE J. Solid-State Circuits* **43** (2008) 1436 (DOI: [10.1109/JSSC.2008.922716](https://doi.org/10.1109/JSSC.2008.922716)).
- [9] B. Analui, *et al.*: “A 10-Gb/s two-dimensional eye-opening monitor in 0.13- μ m standard CMOS,” *IEEE J. Solid-State Circuits* **40** (2005) 2689 (DOI: [10.1109/JSSC.2005.856576](https://doi.org/10.1109/JSSC.2005.856576)).
- [10] H. Noguchi, *et al.*: “A 40-Gb/s CDR circuit with adaptive decision-point control based on eye-opening monitor feedback,” *IEEE J. Solid-State Circuits* **43** (2008) 2929 (DOI: [10.1109/JSSC.2008.2006227](https://doi.org/10.1109/JSSC.2008.2006227)).
- [11] H. Won, *et al.*: “A 28-Gb/s receiver with self-contained adaptive equalization and sampling point control using stochastic sigma-tracking eye-opening monitor,” *IEEE Trans. Circuits Syst. I, Reg. Papers* **64** (2017) 664 (DOI: [10.1109/TCSI.2016.2614349](https://doi.org/10.1109/TCSI.2016.2614349)).
- [12] J. F. Bulzacchelli, *et al.*: “A 10-Gb/s 5-tap DFE/4-tap FFE transceiver 90-nm CMOS technology,” *IEEE J. Solid-State Circuits* **41** (2006) 2885 (DOI: [10.1109/JSSC.2006.884342](https://doi.org/10.1109/JSSC.2006.884342)).
- [13] R. Payne, *et al.*: “A 10-Gb/s 5-tap DFE/4-tap FFE transceiver 90-nm CMOS technology,” *IEEE J. Solid-State Circuits* **40** (2005) 12 (DOI: [10.1109/JSSC.2005.856583](https://doi.org/10.1109/JSSC.2005.856583)).
- [14] S. L. J. Gierkink: “Low-spur, low-phase-noise clock multiplier based on a combination of PLL and recirculating DLL with dual-pulse ring oscillator and self-correcting charge pump,” *IEEE J. Solid-State Circuits* **43** (2008) 2967 (DOI: [10.1109/JSSC.2008.2006225](https://doi.org/10.1109/JSSC.2008.2006225)).
- [15] G. Balamurugan, *et al.*: “A scalable 5–15 Gbps, 14–75 mW low-power I/O transceiver in 65 nm CMOS,” *IEEE J. Solid-State Circuits* **43** (2008) 1010 (DOI: [10.1109/JSSC.2008.917522](https://doi.org/10.1109/JSSC.2008.917522)).
- [16] K. Kaviani, *et al.*: “A tri-modal 20-Gbps/link differential/DDR3/GDDR5 memory interface,” *IEEE J. Solid-State Circuits* **47** (2012) 926 (DOI: [10.1109/JSSC.2012.2185370](https://doi.org/10.1109/JSSC.2012.2185370)).
- [17] J. T. Stonick, *et al.*: “An adaptive PAM-4 5-Gb/s backplane transceiver in 0.25- μ m CMOS,” *IEEE J. Solid-State Circuits* **38** (2003) 436 (DOI: [10.1109/JSSC.2002.808282](https://doi.org/10.1109/JSSC.2002.808282)).
- [18] J. L. Zerbe, *et al.*: “Equalization and clock recovery for a 2.5–10-Gb/s 2-PAM/4-PAM backplane transceiver cell,” *IEEE J. Solid-State Circuits* **38** (2003) 2121 (DOI: [10.1109/JSSC.2003.818572](https://doi.org/10.1109/JSSC.2003.818572)).
- [19] Y. Hidaka, *et al.*: “A 4-channel 1.25–10.3 Gb/s backplane transceiver macro with 35 dB equalizer and sign-based zero-forcing adaptive control,” *IEEE J. Solid-State Circuits* **44** (2009) 3547 (DOI: [10.1109/JSSC.2009.2031021](https://doi.org/10.1109/JSSC.2009.2031021)).
- [20] J. G. Maneatis, *et al.*: “Low-jitter process-independent DLL and PLL based on self-biased techniques,” *IEEE J. Solid-State Circuits* **31** (1996) 1723 (DOI: [10.1109/JSSC.1996.542317](https://doi.org/10.1109/JSSC.1996.542317)).
- [21] J. F. Buckwalter, *et al.*: “Analysis and equalization of data-dependent jitter,” *IEEE J. Solid-State Circuits* **41** (2006) 607 (DOI: [10.1109/JSSC.2005.864119](https://doi.org/10.1109/JSSC.2005.864119)).
- [22] V. Stojanovic, *et al.*: “Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery,” *IEEE J. Solid-State Circuits* **40** (2005) 1012 (DOI: [10.1109/JSSC.2004.842863](https://doi.org/10.1109/JSSC.2004.842863)).
- [23] J. F. Bulzacchelli, *et al.*: “A 10-Gb/s 5-tap DFE/4-tap FFE transceiver in 90-nm CMOS technology,” *IEEE J. Solid-State Circuits* **41** (2006) 2885 (DOI: [10.1109/JSSC.2006.884342](https://doi.org/10.1109/JSSC.2006.884342)).
- [24] S. Galal and B. Razavi: “Broadband ESD protection circuits in 0.18-/spl mu/m CMOS technology,” *IEEE J. Solid-State Circuits* **39** (2004) 2389 (DOI: [10.1109/JSSC.2004.835639](https://doi.org/10.1109/JSSC.2004.835639)).
- [25] K.-L. J. Wong, *et al.*: “A 5-mW 6-Gb/s quarter-rate sampling receiver with a 2-tap DFE using soft decisions,” *IEEE J. Solid-State Circuits* **42** (2007) 881 (DOI: [10.1109/JSSC.2007.892189](https://doi.org/10.1109/JSSC.2007.892189)).
- [26] B. Kim, *et al.*: “A 10-Gb/s compact low-power serial I/O with DFE-IIR equalization in 65-nm CMOS,” *IEEE J. Solid-State Circuits* **44** (2009) 3526 (DOI: [10.1109/JSSC.2009.2031015](https://doi.org/10.1109/JSSC.2009.2031015)).
- [27] T. O. Dickson, *et al.*: “A 12-Gb/s 11-mW half-rate sampled 5-tap decision feedback equalizer with current-integrating summers in 45-nm SOI CMOS technology,” *IEEE J. Solid-State Circuits* **44** (2009) 1298 (DOI: [10.1109/JSSC.2009.2014733](https://doi.org/10.1109/JSSC.2009.2014733)).
- [28] G. E. Zhang and M. M. Green: “A 10 Gb/s BiCMOS adaptive cable equalizer,” *IEEE J. Solid-State Circuits* **40** (2005) 2132 (DOI: [10.1109/JSSC.2005.857354](https://doi.org/10.1109/JSSC.2005.857354)).
- [29] Y. Kudoh, *et al.*: “A 0.13- μ m CMOS 5-Gb/s 10 m 28AWG cable transceiver with no-feedback-loop continuous-time post-equalizer,” *IEEE J. Solid-State Circuits* **38** (2003) 741 (DOI: [10.1109/JSSC.2003.810029](https://doi.org/10.1109/JSSC.2003.810029)).
- [30] J. Sewter and A. C. Carusone: “A 3-tap FIR filter with cascaded distributed tap amplifiers for equalization up to 40 Gb/s in 0.18- μ m CMOS,” *IEEE J. Solid-State Circuits* **41** (2006) 1919 (DOI: [10.1109/JSSC.2006.875293](https://doi.org/10.1109/JSSC.2006.875293)).