Design of a third-order delta-sigma TDC with error-feedback structure

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Abstract: A 1-1-1 MASH delta-sigma TDC with a simpler structure was designed using an error feedback structure. The proposed 1-1-1 MASH delta-sigma TDC modulator has a single subtractor without any explicit integrator. Each modulator stage is composed of a subtractor, digital-to-time converter, and a quantizer. The subtractor generates the timing difference between input signal interval and the feedback signal interval. The digital-to-time converter (DTC) adds or subtracts fixed delays depending on the subtractor output and the quantizer values. The proposed circuit was designed using a 180 nm CMOS process. The simulation results show a resolution of 2.07 ps and a valid bit count of 11.5 bits at a sampling frequency of 50 MHz. The area is 0.14 mm², and the power consumption is 1.34 mW.

Keywords: DSM (delta-sigma modulation), TDC (time-to-digital converter), error-feedback structure modulator

Classification: Integrated circuits

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1 Introduction

High-performance, high-resolution time-to-digital converters (TDCs) are used in a variety of applications, such as all digital phase locked loops (ADPLLs), clock data recovery, and time of flight (TOF) measurements. TOF measurement is to pick up the return time of a light pulse toward a target, which is important in many industrial applications, such as automotive location and particle detection. This requires a precise time-to-digital converter and the accuracy of the TOF is determined by the resolution of TDC. Conventional time-to-digital converters mostly involve delay lines. However, the timing resolution is limited by an absolute delay or relative delay difference in vernier delay line technique [1]. TDCs based on gated ring oscillators were published [2, 3]. The approach needs many numbers of delay stages in ring oscillators. The delta-sigma MASH modulators were investigated for various applications [4, 5]. The delta-sigma TDC approaches were researched for increasing time resolution [6, 7]. Ref. [6] adopted a single loop delta-sigma (DS) TDC using a charge pump circuit as an integrator. It requires a large capacitor in the integrator and a ramp circuit for quantization. Ref. [7] adopted a 1-1-1 MASH delta-sigma TDC with an error feedback. It has two subtractors to realize the error feedback DS modulator. Ref. [8, 9] also uses two subtractors to compose the integrator.

In this paper, we propose a TDC using a delta-sigma modulation (DSM) with error feedback for noise shaping. The proposed a 1-1-1 MASH delta-sigma TDC is designed using a single subtractor compared to two subtractors in other works [7] and does not need any explicit integrator circuit. By the digital-to-time converter (DTC) which adding or subtracting a fixed delay depending on the quantizer values, a subtractor can be saved. Therefore, the TDC structure is simpler and more robust than other works.

2 Architecture

Fig. 1(a) shows a general model of the first order delta-sigma (DS) modulator with the error feedback structure. Fig. 1(b) is a block diagram of the proposed DS TDC. Compared to ref. [7] which also realized DS TDC using the error feedback structure, the proposed DS TDC can be implemented using only one subtractor

Fig. 1. Model of first order DS modulator with error feedback (a), and the block diagram of the proposed first-order DS TDC with error feedback (b)

without any explicit integrator. This is because the digital-to-time converter (DTC) in the feedback path is inherently providing a subtracting action. Thus the circuit can be designed with a simpler structure. And the time integrator function is embedded in the subtractor block.

Since the time subtractor design is the most critical block in the approach, the subtractor design detail is described first. Fig. 2(a) shows the block diagram of the subtractor used in the DS TDC. In order to measure the time in voltage domain, a charge pump circuit is used. The charge pump circuit has a constant current source and sink with two control switches, which are for charging up (PMOS switch) and charging down (NMOS switch), respectively [10]. In order to drive the charge pump block (CP), input and feedback signals and their inverted signals are required. Therefore, a single differential converter (SDC) is inserted at input. The rising edge of input start (In_start) initiates $D F/F_1$ output (Q_In_start) to discharges current from the charge pump block, and lowers the capacitor voltage ($VC1$) that is connected to CP output. When input stop rising edge is received, discharging process is stopped by resetting $D F/F_1$ and $VC1$ is constant. And when the start signal returns to zero, the capacitor voltage is to be discharged further until $VC1$ reaches the logic threshold of the inverter (INV) and the inverter output ($x1$) starts to rise. To charge back the capacitor to its initial value, $x1$ is used as clocking $D F/F_3$. Thus $\bar{Q}$ of $D F/F_3$ becomes '0' and it drives CP to charge the capacitor voltage back to its full level during *Charging_delay* period.

As described, the capacitor voltages ($VC1$, $VC2$) are set initially at the fully charged level and they decreased upon input timing difference. And the voltage level information is converted back to timing information using an inverter (INV). The time for the capacitor voltage change from the fully charged level to the logic threshold of the inverter is defined as T . It depends on the capacitor size, CP current, and charging and discharging time of $VC1$ and $VC2$. In addition, T value can be

Fig. 2. (a) Block diagram of the subtractor, and (b) its operation timing diagram

varied upon input frequency and input timing range to be measured. In this design, the target frequency is set as 50 MHz, thus single conversion process must be done in 20 ns. This determines the charging and discharging current and capacitors' size. The stable controllability on the charging and discharging current determines the accuracy of time subtraction. In charge pump circuit, discharging current is set 11 μ A and is staying very constant within the voltage range between 0.9 V to 1.8 V. This makes the charge pump to flow the current linearly on the voltage change. The capacitor size is 500 fF. The time to take from the fully charges state to the level of logic threshold of INV , which is T , is set as 10 ns in this design and it can be varied upon different applications, such as detecting timing range and sampling frequency. $D F/F_1$ is for generating a signal for discharging the capacitor voltage, and $D F/F_2$ is for additional discharging the capacitor voltage. The two outputs of D

F/F's go through OR gate. When a 1-1-1 MASH structure is built, the second and third stages of DSM have the same structure with the first stage. Since the clock signals of $D\ F/F\_2$ in the second and third stages use the same signal (QB_In_start) as the first stage, the capacitor voltage can be discharged at the same time. Details of multi-stage 1-1-1 MASH structure will be given later in detail.

Fig. 2(b) shows a timing diagram of time subtractor operation. As shown the time difference ($In1 - In2$) between input signal interval ($In1 = In\_start - In\_stop$) and feedback signal interval ($In2 = FB\_start - FB\_stop$) can be measured at the output as $Out\_1 - Out\_2$ as depicted in Fig. 2. The 2nd capacitor's voltage information ($VC2$) is the time interval information of feedback signal interval. Discharging is occurring at the same time as the input and the feedback signal evaluation when In_start goes to zero. As shown in Fig. 2(b), the final subtracted value between two timing value is coming out as T is cancelled.

Fig. 3(a) shows the detailed structure of the proposed first order DSM. One output signal from the subtractor, OUT_1 , goes to input of the quantizer flip-flop, and another output signal, OUT_2 , is used as a clocking for the quantizer flip-flop. Depending on QT_OUT value, an extra delay ($Delay\_3$) is added or not added to OUT_1 and OUT_2 . The value of $Delay\_3$ corresponds to digital '1', which is set as 2 ns in this design. This corresponds to 1-bit DAC in voltage domain modulator. And this is equivalent to 1 bit delay time. The value of $Delay\_3$ can be changed upon design specifications. When OUT_1 signal is ahead of OUT_2 , QT_OUT is '1'. Since OUT_1 and OUT_2 are used for F/F operation, OUT_1 pulse width should be long enough to obtain correct '1' output. To extend the OUT pulses for proper F/F action, the charging up current in the subtractor is controlled. Reducing the charging current for VC means slowing down the VC voltage rising, thus the OUT pulse width can be extended. However, the approach is possible as far as the design constraints are allowed. The operating frequency, measuring input timing range, and the processing time in the subtractor should be considered. For example, if we apply 50 MHz clock frequency, the processing time should be within 20 ns to measure the input timing range of 7 ns. In the case, we can extend the pulse width of OUT_1 and OUT_2 up to 8 ns for catching QT_OUT correctly by controlling the charging current to VC . If the OUT pulses to be extended more to handle a larger input timing range, the extra pulse extending circuit should be added. This requires another F/F and adding delay circuits.

Using the quantizer output value (QT_OUT), the digital time converter (DTC) determines how much OUT_1 or OUT_2 is to be delayed for feedback calculation path. This is equivalent to adding or subtracting 1-bit time. In a case that $QT\_OUT = '1'$, OUT_1 is passed through $Delay\_3$ and is used as a feedback stop signal (FB_stop). When $QT\_OUT = '0'$, OUT_2 is used as FB_start after passing through $Delay\_3$. Fig. 3(b) illustrates the operation when the quantizer output (OUT) is '1' case. In the case, OUT_1 is delayed by $Delay\_3$ compared to OUT_2 , and it is used as a feedback stop signal. OUT_2 serves as a feedback start signal. In this way, the subtraction is executed with outputs of DTC. This saves one subtractor compared to two subtractors used in the conventional approach [7]. The outputs of the subtraction (FB_start_new , FB_stop_new) becomes the next feedback signal to be used. The timing information between FB_start_new and FB_stop_new

Fig. 3. (a) Block diagram of the proposed first order DSM, (b) Timing diagram.

is a quantization error (q_error) from the quantizer. The two outputs of the subtractor (OUT_1 and OUT_2) are commonly delayed by $Delay\_2$ in order to prevent OUT_1 and OUT_2 from entering to MUX input in DTC block before the quantizer output (QT_OUT) reaches DTC. $Delay\_2$ is set to be 5 ns in this design. This value is determined by the quantizer delay and MUX setup time. And considering the total discharging time of 12 ns and $Delay\_2$ of 5 ns, the input measurement range can be 7 ns in this design. Input stop signal and feedback stop signal are additionally delayed by $Delay\_1$ so that the start signals always precede

the stop signals in the last stage DSM. In this design, $Delay\_1$ is set to be 5 ns. Fig. 4 shows a block diagram of the proposed 1-1-1 MASH SD TDC circuit.

Three stages of DSM are placed as shown in Fig. 4. If the input timing to be measured is T_{in} , The input of the second stage is $T_{in} - qerror\_1$, ($qerror$ is quantization error of each quantizer) and input of third stage is $T_{in} - qerror\_1 - qerror\_3$, respectively. The maximum quantization error of a single quantizer in this design is 2 ns, which is determined by $Delay\_3$ that is equivalent to 1 bit time. Since the proposed subtractor should work on a positive value input timing, the third stage input ($T_{in} - (qerror\_1 + qerror\_3)$) must be positive. Therefore we have to compensate the possible worst case of negative value in third stage input, which is two maximum quantization errors ($qerror\_1 + qerror\_3$). $Delay\_1$ (5 ns) offset at the *stop* signal input is given for this after some margin is added. As explained before, $Delay\_2$ is to prevent OUT_1 and OUT_2 from entering to MUX input in DTC block before the quantizer output (QT_OUT) reaches DTC in Fig. 3. $Delay\_2$ is set to be 5 ns in this design. This value is determined by the quantizer delay and MUX setup time. The values of $Delay\_1$ and $Delay\_3$ can be varied on different design specifications, such as different measuring time ranges, timing resolutions, and operating frequencies. However, $Delay\_2$ is only dependent on the quantizer delay and MUX setup time.

Variations of $Delay\_1$, $Delay\_2$, and $Delay\_3$ affect SNR in the signal, which is eventually reflected on ENOB of the TDC. $Delay\_1$ is used for making the input timing in each stage a positive value, as described before, and 1 ns margin is added under the worst quantization error. Therefore, $Delay\_1$'s variation is not affecting the TDC performance. Also, since $Delay\_2$ is used only for the setup timing in the DTC feedback path, the delay variation effect is not visible if enough timing margin is given. The most important delay variation is from $Delay\_3$ which determines 1 bit time of the TDC. However, SNR in the TDC is reflected through the over-sampling ratio (OSR), which is 125 in this design. Thus the delay variation effect from $Delay\_3$ on SNR in the proposed TDC is very limited.

Fig. 4. Block diagram of the proposed 1-1-1 MASH SD TDC

To remove the first and second quantizer errors from the output, a noise cancellation circuit is added. By implementing the noise cancellation block, the output of MASH 1-1-1 TDC is given by

$$D\_OUT = Tin + (1 - z^{-1})^3 \cdot qerror\_3, \quad (1)$$

where $qerror\_3$ is the quantization error in the third stage.

Fig. 5 shows the block diagram of the noise cancellation. The adder in the noise cancellation block is designed with a carry look-ahead adder structure. In order to make the outputs reach at the same time, the logic in the adders has the same number of logic gates. The digital values are D_OUT_1 , D_OUT_2 , and D_OUT_3 , which are the outputs of each stage. Initially, a subtractor is built with a 2-bit adder. The subtraction is performed with a one's complement by delaying the operand. Since the Cin in the adder is set to '1', and a two's complement is performed. D_OUT_2 goes through a 2-bit subtractor, and then two values are added through D_OUT_1 and a 3-bit adder. D_OUT_3 goes through a 2-bit subtractor and a 3-bit subtractor, and then added with D_OUT_1 and D_OUT_2 to obtain the final D_OUT with a 4-bit adder.

Fig. 5. Block diagram of the noise cancellation block

3 Simulation results

The proposed TDC is designed with 180 nm CMOS with 1.8 V supply. The proposed TDC is designed for a sampling rate 50 MHz. Fig. 6 shows the layout of the proposed 1-1-1 MASH TDC.

Fig. 6. The layout of the proposed 1-1-1- MASH TDC

The maximum input time interval variation rate, which is equivalent to input signal bandwidth, is 200 KHz. Fig. 7 shows the FFT results on the input time

interval of 0.77 ns (p-p) at 100 kHz rate input rate. It is shown that noise is shifted with a slope of 60 dB/dec because of the third-order DSM action. SNDR of 71.3 dB is obtained using Matlab calculation from Fig. 7, and the timing resolution is derived as 2.07 ps and 11.5 effective number of bits (ENOB) are achieved. The maximum input bandwidth is 200 kHz and the measurement range is 7 ns. By changing the design parameters, the measurement range can be increased. Table I compares the performance with other DS TDCs published recently. Even considering that our numbers are from simulation results compared to other works' chip measurement results, our time resolution and ENOB still shows good results and it shows a feasibility of the proposed DS TDC.

Fig. 7. The output spectrum of the proposed 1-1-1- MASH TDC

The chip area and power consumption were a little bit larger than others. The reason is the use of relatively large value delays, which leads to a large area and power consumption. The second reason is the usage of 180 nm CMOS process technology. If the delays used in the circuit are appropriately reduced and a better CMOS process is applied, the area and power consumption index could be better.

Table I. Performance comparison with prior works

	This work	[6]	[7]	[8]
Type	3rd order MASH	Single-loop	3 rd order MASH	Single-loop
Technology	180 nm CMOS	110 nm CMOS	130 nm CMOS	90 nm CMOS
Supply Voltage	1.8 V	1.2 V	1.2 V	1.2 V
Sampling rate	50 MS/s	12.8 MS/s	50 MS/s	156 MS/s
Signal BW	200 kHz	50 kHz	100 kHz	1000 kHz
Resolution	2.07 ps	4.7 ps	5.6 ps	2.4 ps
No. of bits	11.5	13	11	10
Measurement range	7 ns	39.06 ns	20 ns	3.2 ns
Total Circuit Area	0.14 mm²	0.11 mm ²	0.11 mm ²	0.12 mm ²
Power	1.34 mW	0.4 mW	1.7 mW	2.1 mW

4 Conclusions

A 1-1-1 MASH delta-sigma TDC with a simpler structure was designed using an error feedback structure. The proposed modulator uses only a single subtractor without any explicit integrator. The proposed circuit was designed using a 180 nm CMOS process. The simulation results show a resolution of 2.07 ps and a valid bit count of 11.5 bits at a sampling frequency of 50 MHz. The area is 0.14 mm², and the power consumption is 1.34 mW.

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