An exponent-scalable method for very small capacitance spread and large time constant of switched-capacitor integrator

Quan Li\textsuperscript{1,2}, Yan Li\textsuperscript{1,2}, Xiaosong Wang\textsuperscript{a}, Xin Liu\textsuperscript{b}, and Yu Liu\textsuperscript{c}

\textsuperscript{1} Beijing Key Laboratory of RFIC Technology for Next Generation Communications, Institute of Microelectronics of Chinese Academy of Sciences, No. 3 Beiducheng West Road, Chaoyang District, Beijing, 100029, China
\textsuperscript{2} University of Chinese Academy of Sciences, No. 19(A) Yuquan Road, Shijingshan District, Beijing, 100049, China
\textsuperscript{a}) wangxiaosong@ime.ac.cn
\textsuperscript{b}) liuxin@ime.ac.cn
\textsuperscript{c}) liuyu5@ime.ac.cn

Abstract: For switched-capacitor (SC) integrator, an exponent-scalable method to obtain very small capacitance spread and large time constant is presented. Based on Nagaraj-89 SC integrator, an additional SC feedback branch with an extra clock phase is employed, resulting in capacitance spread to the 3rd power in z-domain transfer function. Furthermore, with \((N - 2)\) additional SC feedback branches using \((N - 2)\) extra clock phases, capacitance spread to the \(N\)th power can be achieved in z-domain transfer function. Compared with previous SC integrators, this proposed exponent-scalable method is analyzed, and it is verified by simulation that larger time constant can be realized with less capacitor area. Moreover, Monte-Carlo simulation shows low relative standard deviation of time constant is also maintained.

Keywords: switched-capacitor integrator, capacitance spread, time constant

Classification: Integrated circuits

References

1 Introduction

For decades, switched-capacitor (SC) integrators have been widely used for sensors calibration [1], biomedical instrument [2], sigma-delta modulator [3, 4], etc. In high-Q SC filters processing low frequency signal, very small pole-to-sampling frequency ratio is realized by very large time-constant (VLT) SC integrators [5, 6], whose capacitance spread (CS), defined by the ratio of the largest and smallest capacitors, can be very large. Usually the smallest capacitor should be large enough to suppress switch charge injection, clock feedthrough and off-state leakage. To reduce on-chip capacitor area determined by CS while maintaining VLT, many area-efficient techniques have been proposed [4, 5, 6, 7, 8, 9], and they all feature the square of CS in z-domain transfer function. SC integrators with input of voltage divider [4] or T-cell [5] suffer from parasitic, and they need two large capacitors, so does the stray-insensitive integrator in [6]. Based on [6], non-uniform sampling approach in [7] has a tradeoff between total capacitors area and signal bandwidth. Only one large capacitor is needed in Nagaraj-89 VLT SC integrator [8], and the charge-differencing method [9] applied to [8] still has limitation to further reduce CS because of the sensitivity problems. For the case of extremely small pole-to-sampling frequency ratio, these circuits may not be suitable to keep chip area small while maintaining high precision.

In this paper, we propose an exponent-scalable method applied to Nagaraj-89 VLT SC integrator. With \((N - 2)\) additional SC feedback branches using \((N - 2)\) extra clock phases, CS to the \(N\)th power is achieved in z-domain transfer function with only one large capacitor. Especially for achieving extremely large time constant in the case of high sampling frequency, CS and capacitor area are significantly reduced. Moreover, low relative standard deviation of time constant is also maintained.
2 Proposed SC integrators with CS to the 3rd and the Nth power

Fig. 1 illustrates the conventional, Nagaraj-89 [8] and charge-differencing Nagaraj-89 [9] SC integrators, they all use only one large capacitor. Their time constants can be written as follows respectively:

\[ \tau_{1a} = \frac{C_{\text{int}}}{C_1} T_{sw} = CS \times T_{sw} \]  
\[ \tau_{1b} = \frac{C_{\text{int}}}{C_1} \left( \frac{C_2}{C_1} T_{sw} \right) \approx (CS^2) \times T_{sw} \]  
\[ \tau_{1c} = \frac{C_{\text{int}}}{C_1} \left( \frac{C_{2a} + C_{2b}}{C_{2a} - C_{2b}} \right) T_{sw} \approx (CS^2) \times \left( \frac{C_1}{C_{2a} - C_{2b}} \right) T_{sw} \]

in which \( T_{sw} \) is the switch sampling period. For unit-gain frequency below \( f_{\text{unit}} = 1/2\pi\tau = 0.1 \) Hz and sampling frequency \( f_s = 1/T_{sw} = 20 \) KHz which is enough for biomedical signals below 10 KHz [2], CS defined by \( C_{\text{int}}/C_1 \) should be over 31831 in Eq. (1) and still over 178 in Eq. (2). CS can be reduced in Eq. (3) by choosing small \( (C_{2a} - C_{2b}) \), but considering precision, the minimum value is limited to 126 due to variance summing of \( C_{2a} \) and \( C_{2b} \) [9].

To further reduce CS while maintaining high precision, our proposed SC integrator realizing CS to the 3rd power (CS-3) and its non-overlapping clock phases are shown in Fig. 2. Ignoring amplifier’s DC finite gain and input offset, this integrator functions as follows: The SC integrator’s behavior during \((m - 1)T_{sw} < t < mT_{sw}\) is analyzed. The voltage \( V \) at the time point \( t \) is denoted as \( V[t] \). During \( \Phi_1 : (m - 1)T_{sw} < t < (m - 2/3)T_{sw} \), a charge \( C_1 V_{\text{in}}[(m - 2/3)T_{sw}] \) is transferred from \( C_1 \) to \( C_{\text{int}} \) and \( C_{2a} \) is discharged, resulting additional voltage \( (C_1/C_{\text{int}})V_{\text{in}}[(m - 2/3)T_{sw}] \) is sampled by \( C_{2b} \). During \( \Phi_2 : (m - 2/3)T_{sw} < t < (m - 1/3)T_{sw} \), \( C_1 \) withdraws the charge \( C_1 V_{\text{in}}[(m - 2/3)T_{sw}] \) from \( C_{\text{int}} \), while \( C_{2b} \) distributes its additional sampled charge in \( \Phi_1 \) with \( C_{2a} \), and \( C_{2a} \) transfers it to \( C_{\text{int}} \), resulting additional voltage \( (C_1/C_{\text{int}})(C_2/(C_{\text{int}} + C_2))V_{\text{in}}[(m - 2/3)T_{sw}] \) is sampled by \( C_3 \) when \( C_{2a}C_{2b}/(C_{2a} + C_{2b}) = C_2 \). During \( \Phi_3 : (m - 1/3)T_{sw} < t < mT_{sw} \), \( C_{2a} \) withdraws from \( C_{\text{int}} \) the charge transferred to \( C_{\text{int}} \) in \( \Phi_2 \), while \( C_3 \) distributes its additional sampled charge in \( \Phi_2 \) with \( C_{\text{int}} \). It can be derived that from \( V_{\text{in}} \) to \( V_{\text{out}} \) the z-domain transfer function of this integrator is given by

\[ \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{1 + \frac{T_{sw}}{\tau_{1a}}} \]
The unit gain frequency and time constant of this integrator are approximately given as follows respectively:

\[
 f_{\text{unit}} = \frac{1}{2\pi} \frac{C_1}{C_{\text{int}} + C_2} \frac{C_2}{C_{\text{int}} + C_3} \frac{C_3}{1 - z^{-1}} \approx \frac{1}{2\pi} (CS)^3 \frac{1}{1 - z^{-1}} \quad (5)
\]

\[
 \tau = \frac{C_{\text{int}}}{C_1} \frac{C_{\text{int}} + C_2}{C_2} \frac{C_{\text{int}} + C_3}{C_3} T_{\text{sw}} \approx (CS)^3 \times T_{\text{sw}} \quad (6)
\]

Eq. (5) shows that the minimum CS can be reduced significantly to about 32 for \( f_{\text{unit}} < 0.1 \) Hz when \( f_s = 20 \) KHz. Because only one large capacitor \( C_{\text{int}} \) is used, the chip can be really area-efficient. The optional clock phases generation circuit is shown in Fig. 3.

Fig. 4 illustrates the proposed exponent-scalable SC integrator realizing CS to the \( N \)th power (CS-N), and its clock phases can be generated by extending the circuit in Fig. 3. For \( C_{k,a}C_{k,b}/(C_{k,a} + C_{k,b}) = C_k; \ 1 < k < N \), from \( V_{\text{in}} \) to \( V_{\text{out}} \), CS-N’s z-domain transfer function, unit gain frequency and time constant are approximately given as follows respectively:

\[
 H(z) = \frac{V_{\text{out}}(z)}{V_{\text{in}}(z)} = -\frac{C_1}{C_{\text{int}}} \frac{C_2}{C_{\text{int}} + C_2} \frac{C_3}{C_{\text{int}} + C_3} \frac{z^{-2/3}}{1 - z^{-1}} \approx -\frac{1}{(CS)^3} \frac{z^{-2/3}}{1 - z^{-1}} \quad (7)
\]

\[
 f_{\text{unit}} = \frac{f_s}{2\pi} \frac{C_1}{C_{\text{int}}} \frac{1}{N} \frac{C_k}{C_{\text{int}} + C_k} \sum_{k \neq 1}^{N} \approx \frac{1}{2\pi} (CS)^N f_s \quad (8)
\]

\[
 \tau = T_{\text{sw}} \frac{C_{\text{int}}}{C_1} \left( \frac{C_{\text{int}}}{C_k} + \frac{C_k}{C_{\text{int}}} \right) \approx (CS)^N \times T_{\text{sw}} \quad (9)
\]

It can be seen that CS-2 is the same as Nagaraj-89. Theoretically, CS can approach to 1 by increasing \( N \). It is noted that increasing \( N \) increases the circuit complexity and the chip area may not be reduced any more.
3 Simulation results and comparison

For comparison, the amplifier is designed with DC gain of 60 dB and enough bandwidth. Using the gain- and offset-compensated structure in [10], the SC integrators in Fig. 1b, Fig. 1c, Fig. 2 (CS-3) and with CS to the 4th power (CS-4) were simulated. Switch clock frequency is 20 KHz. The simulated transfer responses are plotted in Fig. 5. It is suggested from Fig. 5 that CS-3 with CS of 40 is sufficient to save much chip area for $f_{\text{unit}} < 0.05$ Hz. CS-4 can further reduce CS.
and unit gain frequency, but even with the gain- and offset-compensated structure, its low-frequency gain is lower and phase error is larger. Higher CS-N can be used when the amplifier’s DC gain is larger.

For TSMC 0.18-µm CMOS process, the smallest capacitor $C_1$ set as 120 fF can have relative standard deviation of 0.18%. Including all capacitors’ mismatch, the four types of SC integrators were simulated with 1000-time Monte-Carlo. Table I lists the circuit parameters and relative standard deviation of time constants for Fig. 5. It can be shown that CS-3 and CS-4 use much less total capacitance than Nagaraj-89 VLT SC integrator while holding close precision level.

Table I. Summary of circuit parameters and relative standard deviation of time constants for Fig. 5 ($f_s = 20$ KHz).

<table>
<thead>
<tr>
<th>Structure</th>
<th>Total capacitance</th>
<th>$\mu(f_{\text{unit}})$</th>
<th>$\mu(t)$</th>
<th>$\sigma(t)/\mu(t)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nagaraj-89 [8]</td>
<td>$202C_1$</td>
<td>0.079 Hz</td>
<td>2.01 s</td>
<td>0.25%</td>
</tr>
<tr>
<td>Charge-differencing  [9]</td>
<td>$153.5C_1$</td>
<td>0.070 Hz</td>
<td>2.29 s</td>
<td>0.59%</td>
</tr>
<tr>
<td>Proposed CS-3</td>
<td>$46C_1$</td>
<td>0.047 Hz</td>
<td>3.36 s</td>
<td>0.26%</td>
</tr>
<tr>
<td>Proposed CS-4</td>
<td>$30C_1$</td>
<td>0.017 Hz</td>
<td>9.26 s</td>
<td>0.30%</td>
</tr>
</tbody>
</table>

4 Conclusion

We have proposed and analyzed an exponent-scalable method for further smaller CS and larger time constant of SC integrator. With $(N - 2)$ additional SC feedback branches using $(N - 2)$ extra clock phases applied to Nagaraj-89 VLT SC integrator, a SC integrator with CS to the $N$th power in $z$-domain transfer function (CS-N) has been realized by using only one large capacitor. The proposed SC integrators as CS-3 and CS-4 have been simulated and compared with Nagaraj-89 (CS-2). It is
verified that especially for achieving extremely large time constant in the case of high sampling frequency, CS and capacitor area are significantly reduced. Moreover, Monte-Carlo simulation shows low relative standard deviation of time constant is also maintained.